TFA9890

9.5 V boosted audio system with adaptive sound maximizer and speaker protection

Rev. 01 — 17 May 2013 Preliminary short data sheet

1. General description

The TFA9890 is a high efficiency class-D audio amplifier with a sophisticated speaker boost and protection algorithm. It can deliver 7.2 W peak output power into an 8 Ω speaker at a supply voltage of 3.6 V. The internal boost converter raises the supply voltage to 9.5 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9890 maximizes acoustic output while ensuring diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker.

Unlike competing solutions, the adaptive sound maximizer algorithm uses feedback to accurately calculate both the temperature and the excursion, allowing the TFA9890 to adapt to changes in the acoustic environment.

Internal intelligent DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The TFA9890 also incorporates advanced battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system undervoltage. The advanced processor minimizes the impact of a falling battery voltage on the audio quality by preventing distortion as the battery discharges.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The audio input interface is I^2S and the control settings are communicated via an I^2C-bus interface.

The device also provides the speaker with robust protection against ESD damage. In a typical application, no additional components are needed to withstand a 15 kV discharge on the speaker.

The TFA9890 is available in a 49-bump WLCSP (Wafer Level Chip-Size Package) with a 400 μm pitch.

2. Features and benefits

- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee or porting required
  - Total integrated solution that includes DSP, amplifier, DC-to-DC, sensing and more
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Output power: 3.6 W (RMS) into 8 Ω at 3.6 V supply voltage (THD = 1 %)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Compatible with standard Acoustic Echo Cancellers (AECs)
- High efficiency and low power dissipation
- Wide supply voltage range (fully operational from 3 V to 5.5 V)
- Two I^2S inputs to support two audio sources
- I^2C-bus control interface (400 kHz)
- Dedicated speech mode with speech activity detector
- Speaker current and voltage monitoring (via the I^2S-bus) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz to 48 kHz supported
- 3 bit clock/word select ratios supported (32x, 48x, 64x)
- Option to route I^2S input direct to I^2S output to allow a second I^2S output slave device to be used in combination with the TFA9890
- TDM interface supported (with limited functionality)
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- 15 kV system-level ESD protection without external components
- ‘Pop noise' free at all mode transitions

3. Applications

- Mobile phones
- Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- MP3 players and portable media players
- Small audio systems

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	3	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive Boost mode (no output signal, V_{BAT} = 3.6 V, V_{DDD} = 1.8 V)	-	4	-	mA
		Power-down mode	-	1	-	μA
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost Protection activated	-	20	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed	-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V	-	10	-	μA
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 0				
		R_L = 8 Ω; f_s = 48 kHz	-	3.6	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	3.7	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9890UK	WLCSP49	wafer level chip-size package; 49 bumps	TFA9890UK

6. Block diagram

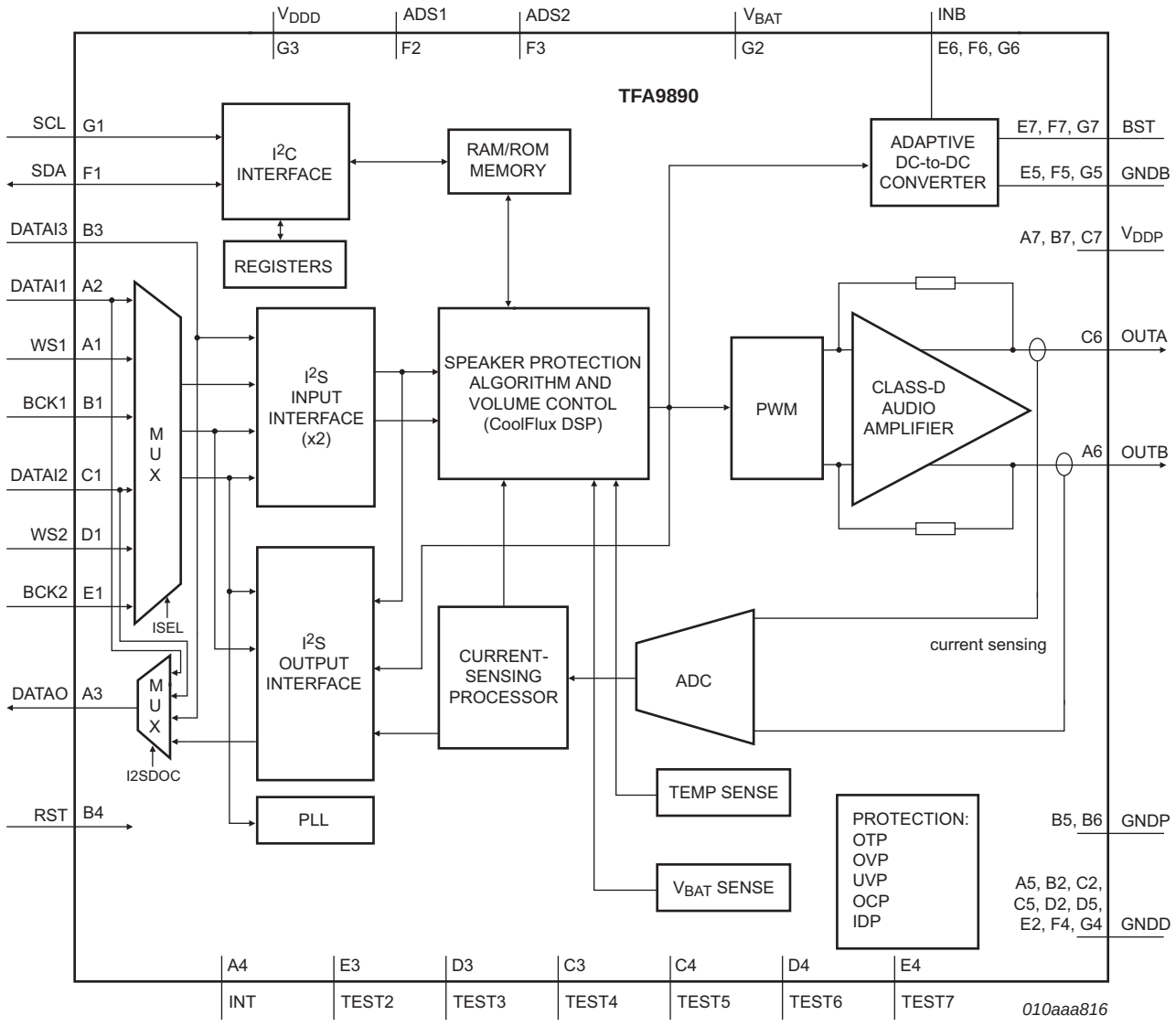
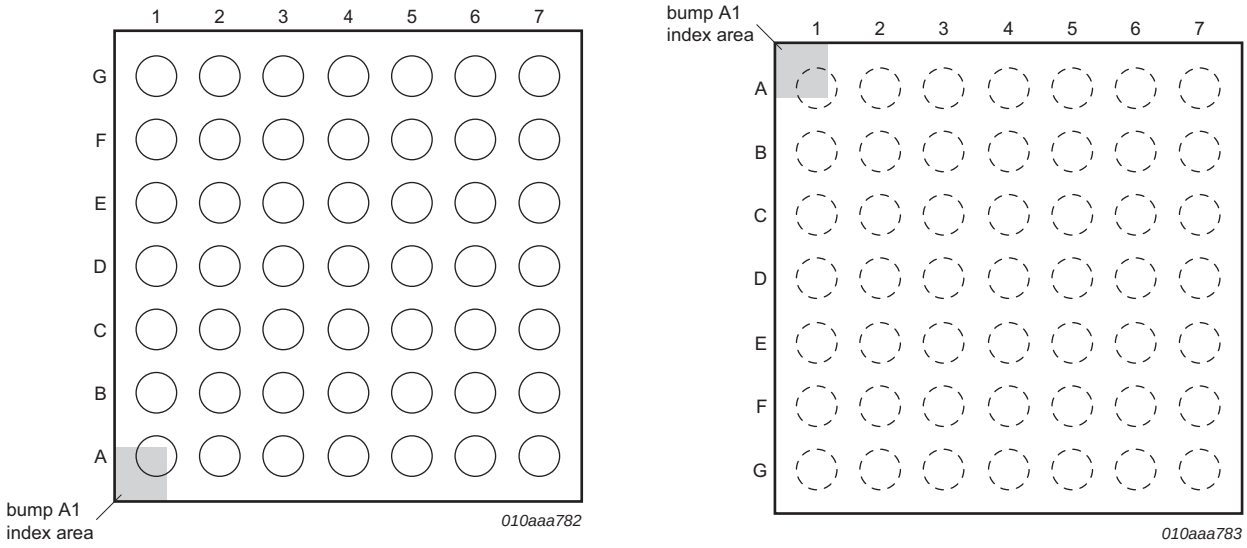


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



a. Bottom view

b. Transparent top view

Fig 2. Bump configuration

	1	2	3	4	5	6	7
A	WS1	DATAI1	DATAO	INT	GNDD	OUTB	V_{DDP}
B	BCK1	GNDD	DATAI3	RST	GNDP	GNDP	V_{DDP}
C	DATAI2	GNDD	TEST4	TEST5	GNDD	OUTA	V_{DDP}
D	WS2	GNDD	TEST3	TEST6	GNDD	n.c.	n.c.
E	BCK2	GNDD	TEST2	TEST7	GNDB	INB	BST
F	SDA	ADS1	ADS2	GNDD	GNDB	INB	BST
G	SCL	V_{BAT}	V_{DDD}	GNDD	GNDB	INB	BST

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Transparent top view

Fig 3. Bump mapping

Table 3. Pinning

Symbol	Pin	Type	Description
WS1	A1	I	digital audio word select input 1
DATAI1	A2	I	digital audio data input 1
DATAO	A3	O	digital audio data output
INT	A4	O	interrupt output
GNDD	A5	P	digital ground
OUTB	A6	O	inverting output
V_{DDP}	A7	P	power supply voltage
BCK1	B1	I	digital audio bit clock input 1
GNDD	B2	P	digital ground
DATAI3	B3	I	digital audio data input 3
RST	B4	I	reset input
GNDP	B5	P	power ground
GNDP	B6	P	power ground
V_{DDP}	B7	P	power supply voltage
DATAI2	C1	I	digital audio data input 2
GNDD	C2	P	digital ground
TEST4	C3	O	test signal input 4; for test purposes only, connect to PCB ground
TEST5	C4	O	test signal input 5; for test purposes only, connect to PCB ground
GNDD	C5	P	digital ground
OUTA	C6	O	non-inverting output
V_{DDP}	C7	P	power supply voltage
WS2	D1	I	digital audio word select input 2
GNDD	D2	P	digital ground
TEST3	D3	O	test signal input 3; for test purposes only, connect to PCB ground
TEST6	D4	O	test signal input 6; for test purposes only, connect to PCB ground
GNDD	D5	P	digital ground
n.c.	D6	-	not connected[1]
n.c.	D7	-	not connected[1]
BCK2	E1	I	digital audio bit clock input 2
GNDD	E2	P	digital ground
TEST2	E3	O	test signal input 2; for test purposes only, connect to PCB ground
TEST7	E4	O	test signal input 7; for test purposes only, connect to PCB ground
GNDB	E5	P	boosted ground
INB	E6	P	DC-to-DC boost converter input
BST	E7	O	boosted supply voltage output
SDA	F1	I/O	I^2C-bus data input/output
ADS1	F2	I	address select input 1
ADS2	F3	I	address select input 2
GNDD	F4	P	digital ground
GNDB	F5	P	boosted ground
INB	F6	P	DC-to-DC boost converter input

Table 3. Pinning *…continued*

Symbol	Pin	Type	Description
BST	F7	O	boosted supply voltage output
SCL	G1	I	I^2C-bus clock input
V_{BAT}	G2	P	battery supply voltage sense input
V_{DDD}	G3	P	digital supply voltage
GNDD	G4	P	digital ground
GNDB	G5	P	boosted ground
INB	G6	P	DC-to-DC boost converter input
BST	G7	O	boosted supply voltage output

[1] Can be used to simplify routing to OUTA (see Figure 3).

8. Functional description

The TFA9890 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. Figure 1 is a block diagram of the TFA9890.

It contains three I^2S input interfaces and one I^2S output interface. One of I^2S inputs DATAI1 and DATAI2 can be selected as the audio input stream. The third I^2S input, DATAI3, is provided to support stereo applications. A 'pass-through' option allows one of the I^2S input interfaces to be connected directly to the I^2S output. The pass-through option is provided to allow an I^2S output slave device (e.g. a CODEC), connected in parallel with the TFA9890, to be routed directly to the audio host via the I^2S output.

The I^2S output signal on DATAO can be configured to transmit the DSP output signal, amplifier output current information, DATAI3 Left or Right signal information or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

A SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ±10 °C. Furthermore, advanced signal processing ensures the audio quality remains acceptable at all times.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

Output sound pressure levels are boosted within given mechanical, thermal and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality music in quiet environments.

The frequency response of the TFA9890 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

At low battery voltage levels, the gain is automatically reduced to limit battery current. The output volume can be controlled by the SpeakerBoost protection algorithm or by the host application (external). In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to Follower mode ($V_{BST} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage.

9. Internal circuitry

Table 4. Internal circuitry

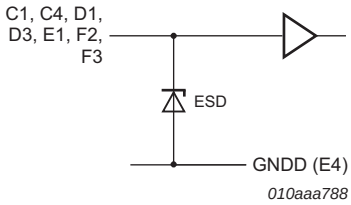
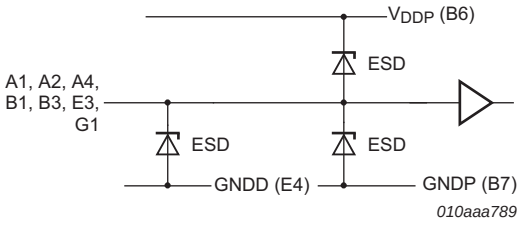
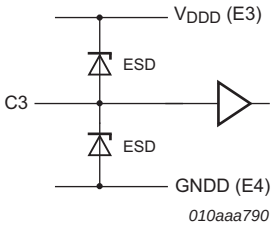
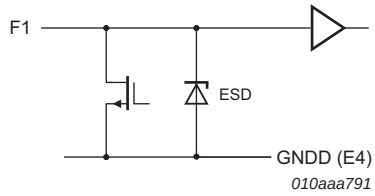
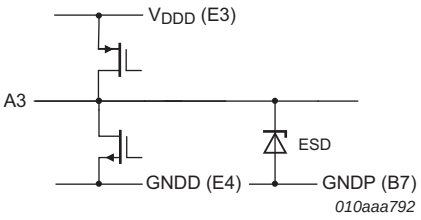
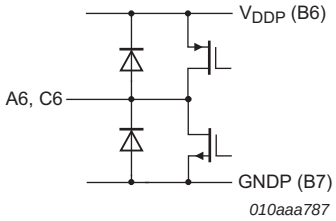
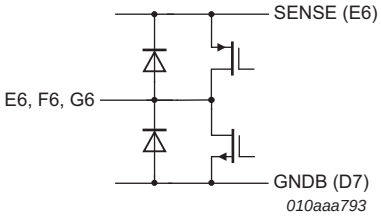
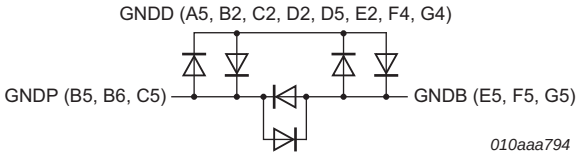
Pin	Symbol	Equivalent circuit
C1, C4, D1, D3, E1, F2, F3	DATAI2, TEST5, WS2, TEST3, BCK2, ADS1, ADS2	
A1, A2, A4, B1, B3, E3, G1	WS1, DATAI1, INT, BCK1, DATAI3, TEST2, SCL,	
C3	TEST4	
F1	SDA	
A3	DATAO	

Table 4. Internal circuitry

Pin	Symbol	Equivalent circuit
A6, C6	OUTB, OUTA	
E6, F6, G6	i.c.	
A5, B2, B5, B6, C2, C5, D2, D5, E2, E5, F4, F5, G4, G5	GNDP, GNDB, GNDD	

10. I²C-bus interface and register settings

The TFA9890 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA9890 and to transmit and receive data. The TFA9890 can only operate in I²C slave mode, as a slave receiver or as a slave transmitter.

10.1 TFA9890 addressing

The TFA9890 is accessed via an 8-bit code (see Table 5). Bits 1 to 7 contain the device address. Bit 0 (R/$\overline{W}$) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address, as detailed in Table 5. The generic address is independent of pins ADS1 and ADS2.

Table 5. Address selection via pins ADS1 and ADS2

ADS2 pin voltage (V)	ADS1 pin voltage (V)	Address	Function
0	0	01101000	for write mode
		01101001	for read mode
0	V_{DDD}	01101010	for write mode
		01101011	for read mode
V_{DDD}	0	01101100	for write mode
		01101101	for read mode
V_{DDD}	V_{DDD}	01101110	for write mode
		01101111	for read mode
don't care	don't care	00011100 (generic address)	for write mode
don't care	don't care	00011101 (generic address)	for read mode

11. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	–0.3	+5.5	V
V_{BST}	voltage on pin BST		–0.3	+12	V
V_{DDP}	power supply voltage	on pin V_{DDP}	–0.3	+12	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	–0.3	+1.95	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	–2	+2	kV
		according to Charge Device Model (CDM)	–500	+500	V

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; natural convection	-	
		4-layer application board	40	K/W

13. Characteristics

13.1 DC Characteristics

Table 8. DC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}		3	-	5.5	V
I_{BAT}	battery supply current	on pin V_{BAT} and in DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive Boost mode (no output signal, V_{BAT} = 3.6 V, V_{DDD} = 1.8 V)		-	4	-	mA
		Power-down mode		-	1	5	µA
V_{DDP}	power supply voltage	on pin V_{DDP}		3	-	9.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		1.65	1.8	1.95	V
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost Protection activated		-	20	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed		-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V		-	10	-	µA
Pins BCK1, WS1, DATA1, BCK2, WS2, DATAI2, DATAI3, ADS1, ADS2, SCL, SDA							
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	3.6	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDD}$	V
C_{in}	input capacitance		[2]	-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin		-	-	0.1	µA
Pins DATAO, INT, push-pull output stages							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} − 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open drain outputs, external 10 kΩ resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		-	-	V_{DDD} − 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins OUTA, OUTB							
R_{DSon}	drain-source on-state resistance	V_{DDP} = 5.3 V		-	200	-	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	150	°C
$V_{ovp(VBAT)}$	overvoltage protection voltage on pin VBAT			5.5	-	6.0	V
$V_{uvp(VBAT)}$	undervoltage protection voltage on pin VBAT			2.3	-	2.5	V

Table 8. DC characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(ocp)}$	overcurrent protection output current		2	-	-	A
DC-to-DC converter						
V_{BST}	voltage on pin BST	DCVO = 111; Boost mode	9.4	9.5	9.6	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).

[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

13.2 AC characteristics

Table 9. AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 0					
		R_L = 8 Ω; f_s = 48 kHz		-	3.6	-	W
		R_L = 8 Ω; f_s = 32 kHz		-	3.7	-	W
		THD+N = 10 %; CLIP = 0					
		R_L = 8 Ω; f_s = 48 kHz		-	4.5	-	W
		R_L = 8 Ω; f_s = 32 kHz		-	4.6	-	W
Amplifier output; pins OUTA and OUTB							
$\lvert V_{O(offset)} \rvert$	output offset voltage	absolute value		-	-	3	mV
Amplifier performance							
η_{po}	output power efficiency	$P_{o(RMS)}$ = 2.5 W; including DC-to-DC converter; 100 Hz audio signal	[2]	-	72	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW; R_L = 8 Ω; L_L = 44 µH	[1]	-	0.03	0.1	%
$V_{n(o)}$	output noise voltage	A-weighted; DATAI1 = DATAI2 = 0 V					
		CoolFlux DSP bypassed		-	50	-	µV
		CoolFlux DSP enabled	[2]	-	66	-	µV
S/N	signal-to-noise ratio	V_O = 4.5 V (peak); A-weighted					
		CoolFlux DSP bypassed		-	100	-	dB
		CoolFlux DSP enabled	[2]	-	97	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV (RMS); f_{ripple} = 217 Hz		-	75	-	dB
f_{sw}	switching frequency	directly coupled to the I^2S input frequency		256	-	384	kHz
Amplifier power-up, power-down and propagation delays							
$t_{d(on)}$	turn-on delay time	PLL locked on BCK (IPLL = 0)					
		f_s = 8 kHz to 48 kHz		-	-	2	ms
		PLL locked on WS (IPLL = 1)					
		f_s = 8 kHz		-	-	27	ms
		f_s = 48 kHz		-	-	6	ms
$t_{d(off)}$	turn-off delay time			-	-	10	µs
$t_{d(mute\_off)}$	mute off delay time			-	1	-	ms
$t_{d(soft\_mute)}$	soft mute delay time			-	1	-	ms
t_{PD}	propagation delay	CoolFlux bypassed					
		f_s = 8 kHz		-	-	3.2	ms
		f_s = 48 kHz		-	-	600	µs
		SpeakerBoost protection mode, $t_{LookAhead}$ = 2 ms					
		f_s = 8 kHz		-	-	14	ms
		f_s = 48 kHz		-	-	4	ms

Table 9. AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Current-sensing performance							
S/N	signal-to-noise ratio	I_O = 1.2 A (peak); A-weighted		-	75	-	dB
$I_{sense(acc)}$	sense current accuracy	I_O = 0.5 A (peak)		−3	-	+3	%
B	bandwidth		[2]	-	8	-	kHz
L_L	load inductance			20	-	-	µH

[1] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).

[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

13.3 I²S timing characteristics

Table 10. I²S bus interface characteristics; see Figure 4

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	on pin WS	[2]	8	-	48	kHz
f_{clk}	clock frequency	on pin BCK	[2]	$32f_s$	-	$64f_s$	Hz
t_{su}	set-up time	WS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] The I²S bit clock input (BCK) is used as a clock input for the DSP, as well as for the amplifier and the DC-to-DC converter. Note that both the BCK and WS signals must be present for the clock to operate correctly.

[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

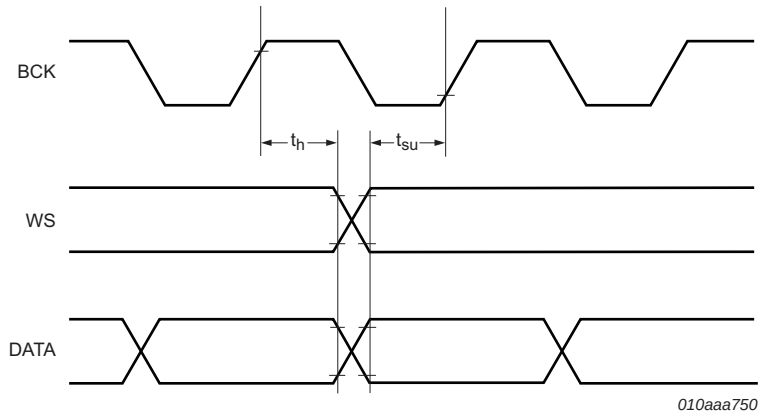


Fig 4. I²S timing

13.4 I²C timing characteristics

Table 11. I²C-bus interface characteristics; see Figure 5

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 9.5 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 40 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

[3] After this period, the first clock pulse is generated.

[4] To be suppressed by the input filter.

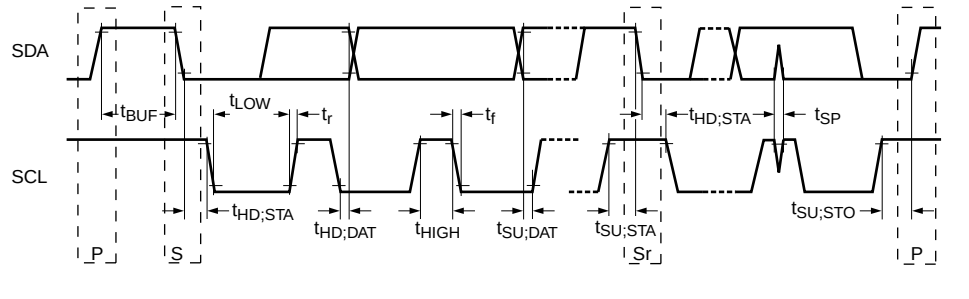


Fig 5. I²C timing

14. Application information

14.1 Application diagrams

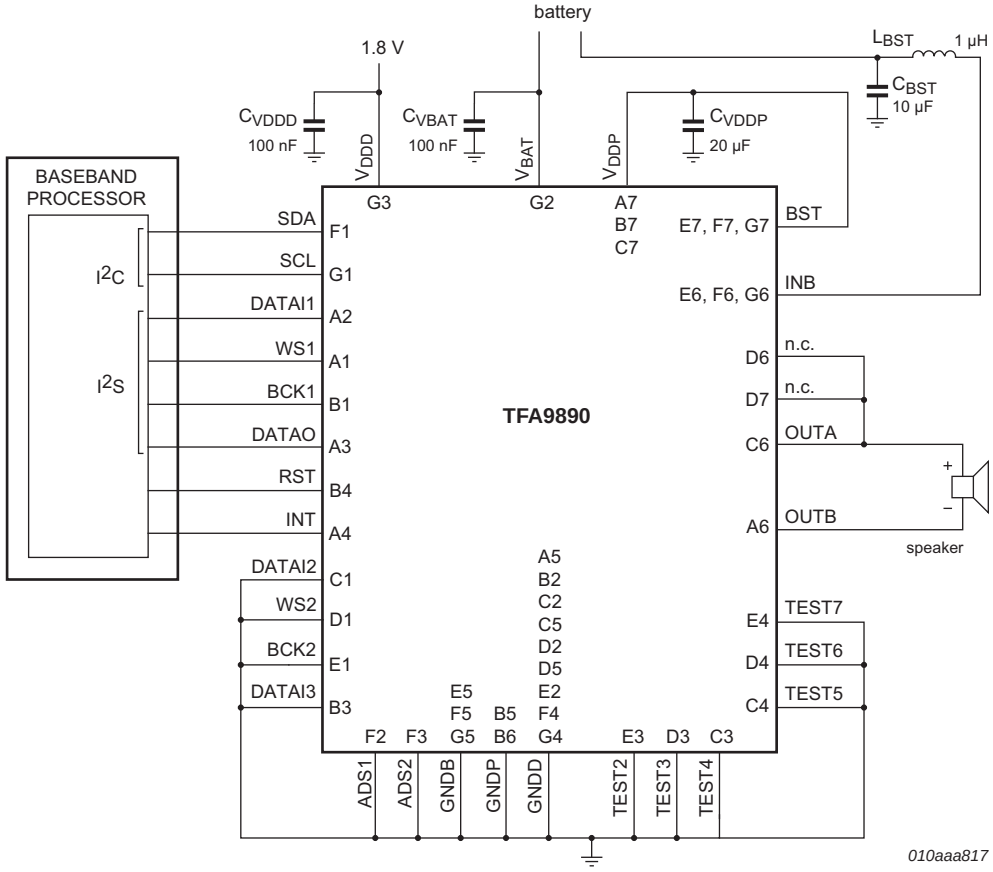


Fig 6. Typical mono application (simplified)

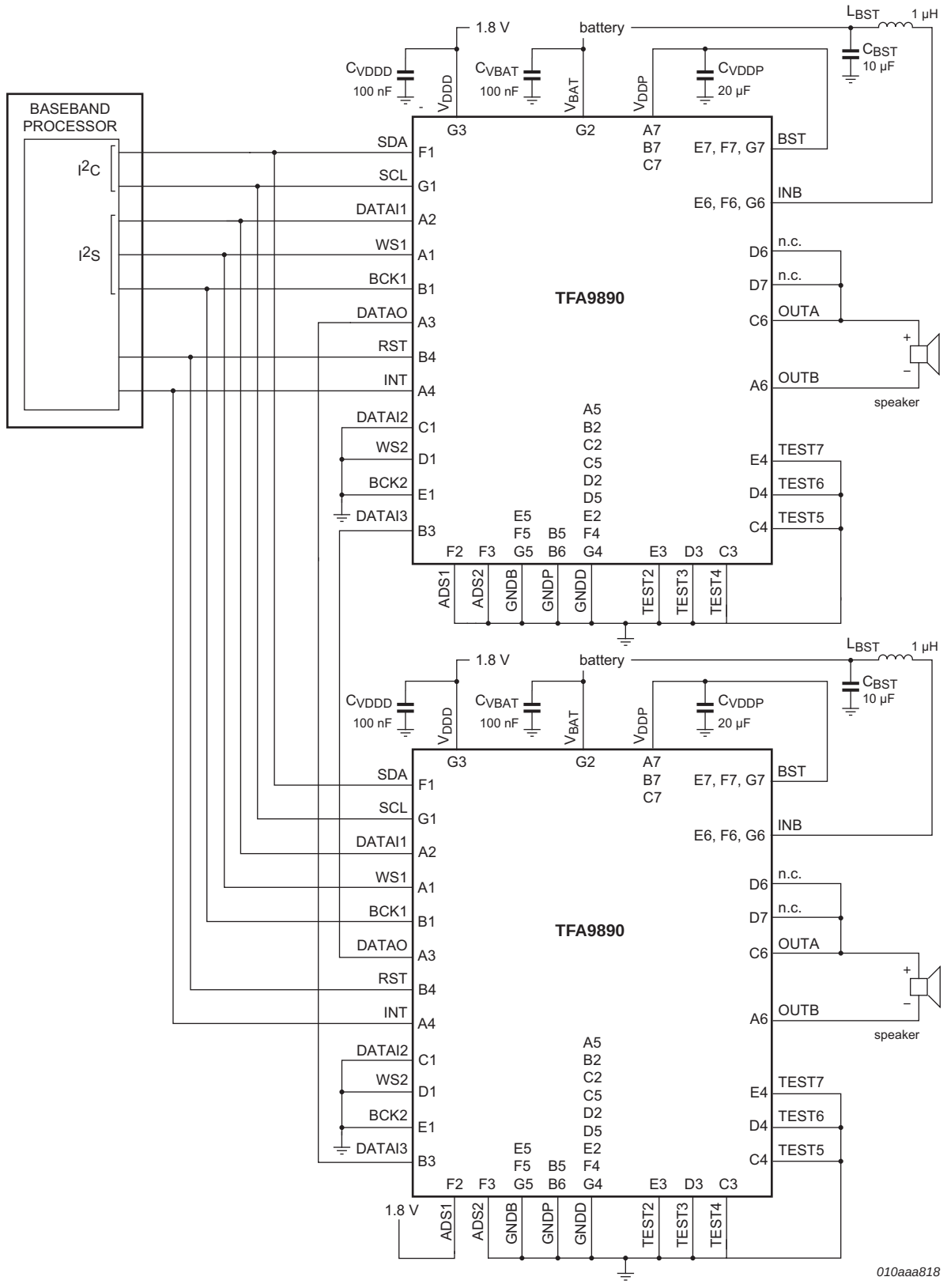


Fig 7. Typical stereo application (simplified)

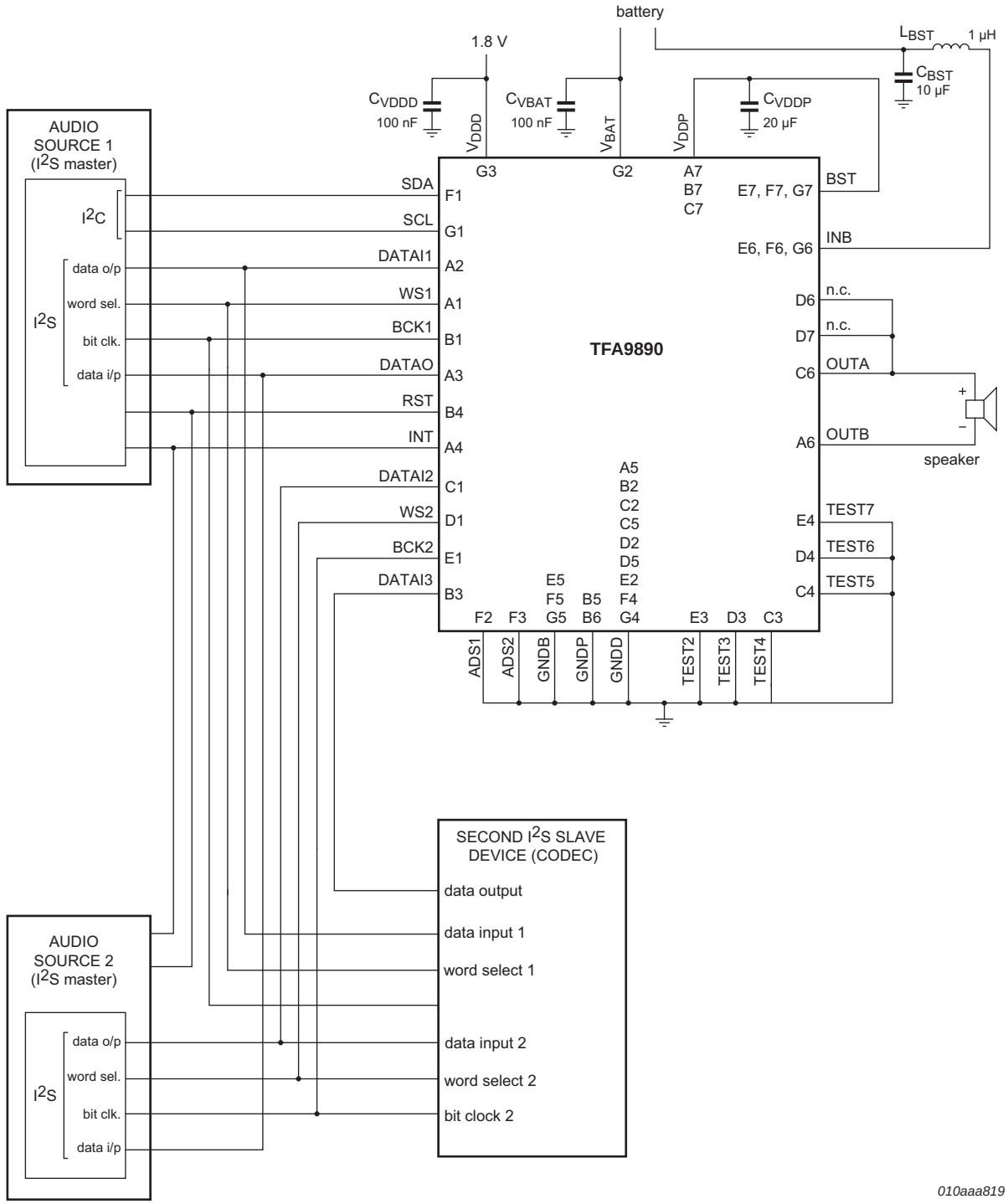
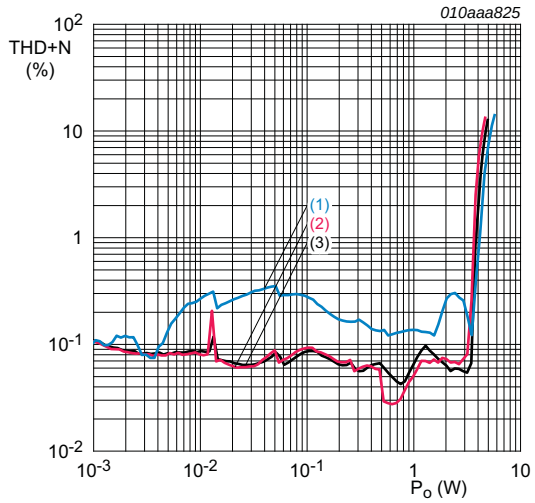


Fig 8. Typical mono application with two audio sources and a second I²S slave device

14.2 Curves measured in reference design (demonstration board)

All measurements were taken with V_{BAT} = *3.6 V;* V_{DDD} = *1.8 V;* V_{DDP} = V_{BST} = *5.3 V;* L_{BST} = *1 µH;* R_L = *4 Ω;* L_L = *20 µH;* f_i = *1 kHz;* f_s = *48 kHz;* T_{amb} = *25 °C; CoolFlux DSP bypassed; default settings, unless otherwise specified.*



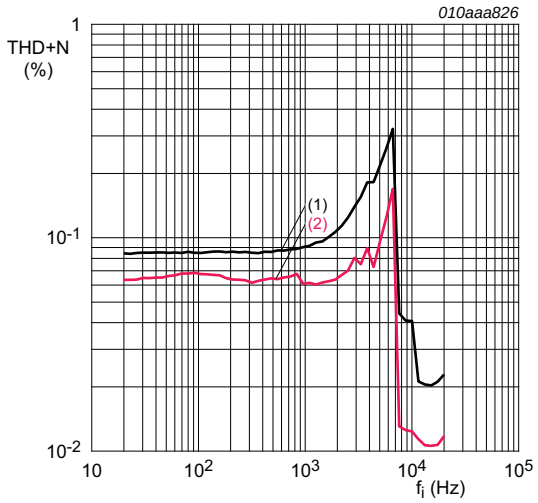
R_L = 8 Ω, V_{BAT} = 3.6 V

(1) f_i = 6 kHz.

(2) f_i = 1 kHz.

(3) f_i = 100 Hz.

Fig 9. THD plus noise as a function of output power

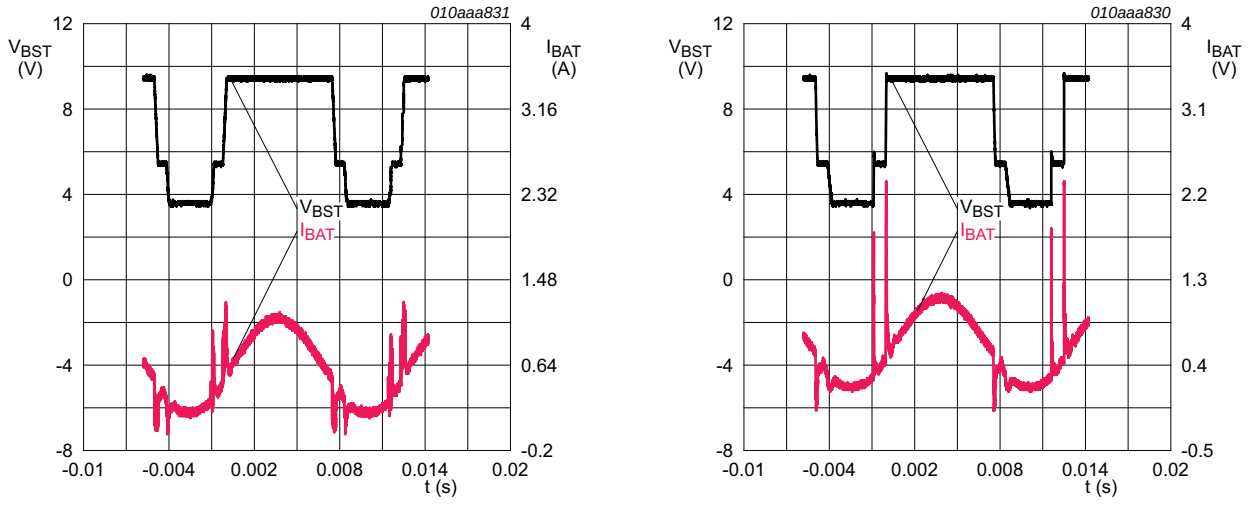


R_L = 8 Ω, V_{BAT} = 3.6 V

(1) P_o = 100 mW

(2) P_o = 500 mW

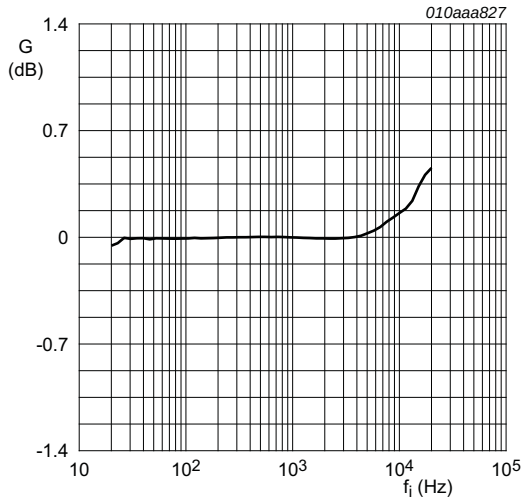
Fig 10. THD plus noise as a function of frequency



a. fast ramp-up

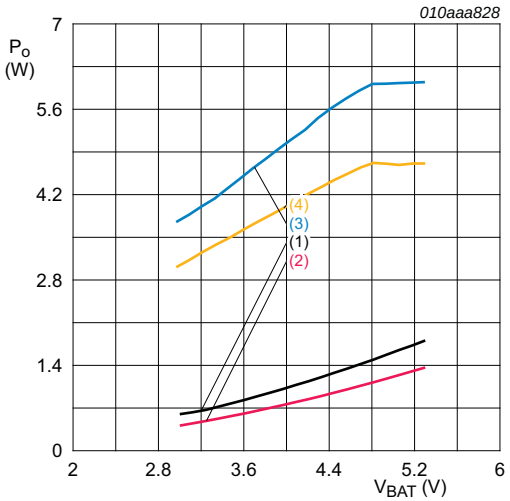
b. immediate ramp-up

Fig 11. DC-to-DC converter ramp-up behavior



R_L = 8 Ω, V_{BAT} = 3.6 V, P_o = 500 mW

Fig 12. Normalized gain as a function of frequency



R_L = 8 Ω, f_i = 1 kHz

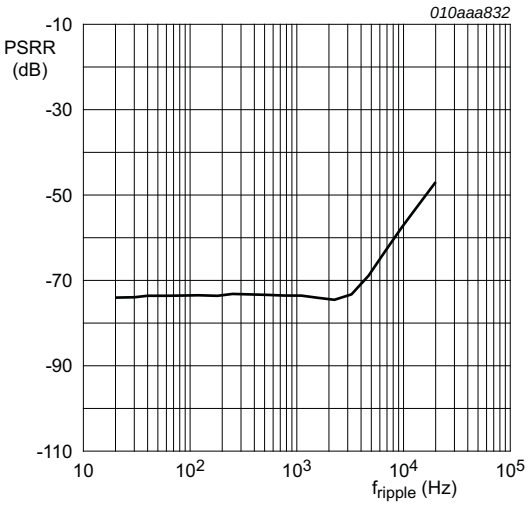
(1) THD+N = 10 %, no boost (Follower mode)

(2) THD+N = 1 %, no boost (Follower mode)

(3) THD+N = 10 %, boost on

(4) THD+N = 1 %, boost on

Fig 13. Output power as a function of battery supply voltage

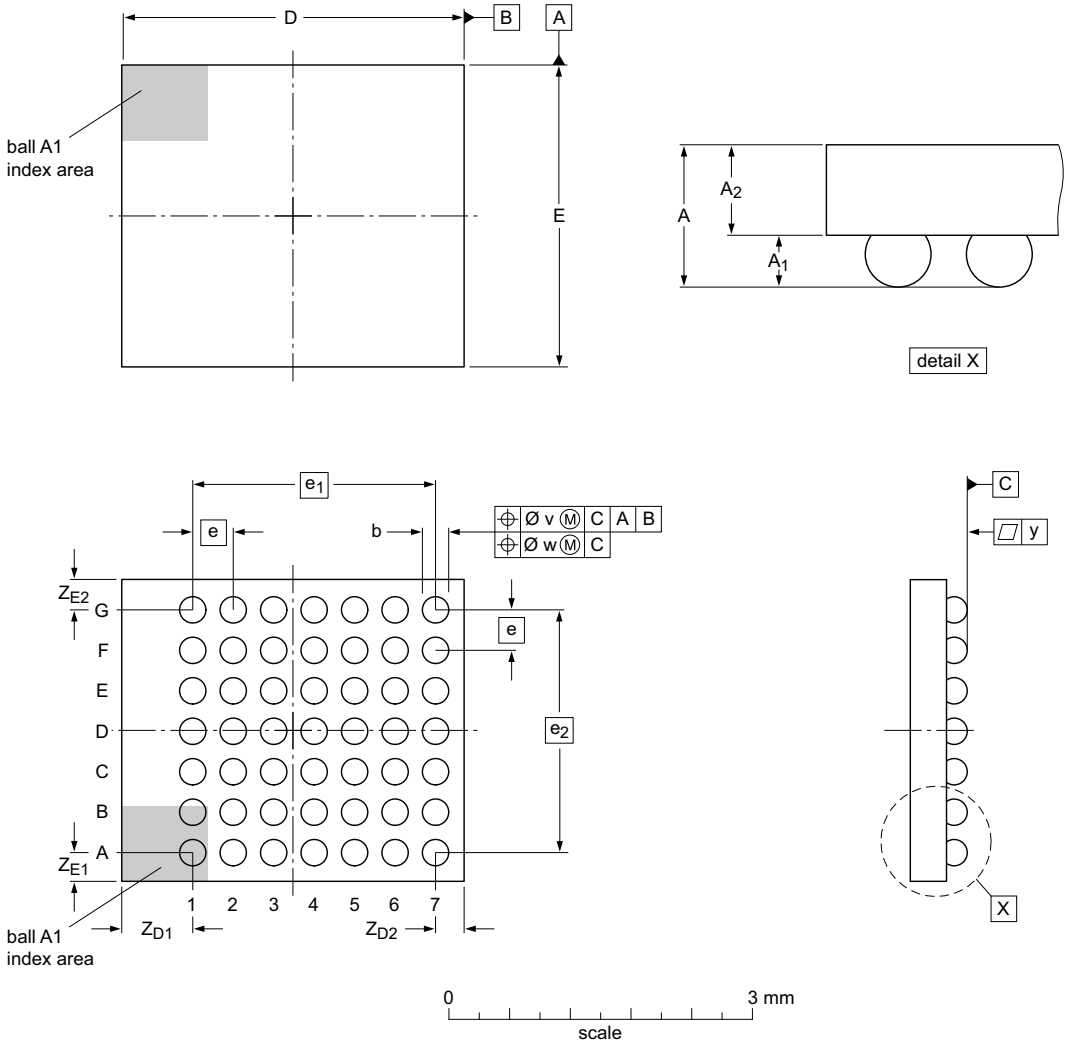


R_L = 8 Ω, V_{BAT} = 3.6 V, V_{ripple} = 200 V(RMS) on V_{BAT}

Fig 14. PSRR as a function of ripple frequency

15. Package outline

WLCSP49: wafer level chip-size package;
49 bumps; 3.37 x 2.97 mm **TFA9890**



Dimensions (mm are the original dimensions)

Unit		Amax	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}
	max	0.6	0.22	0.38	0.28	3.40	3.00							0.725	0.305	0.305	0.325
mm	nom		0.20	0.36	0.26	3.37	2.97	0.4	2.4	2.4	0.015	0.04	0.02	0.695	0.275	0.275	0.295
	min		0.18	0.34	0.24	3.34	2.94							0.665	0.245	0.245	0.265

wlcsp49_tfa9890_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFA9890						~~13-03-07~~ 13-05-17

Fig 15. Package outline TFA9890 (WLCSP49)

16. Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

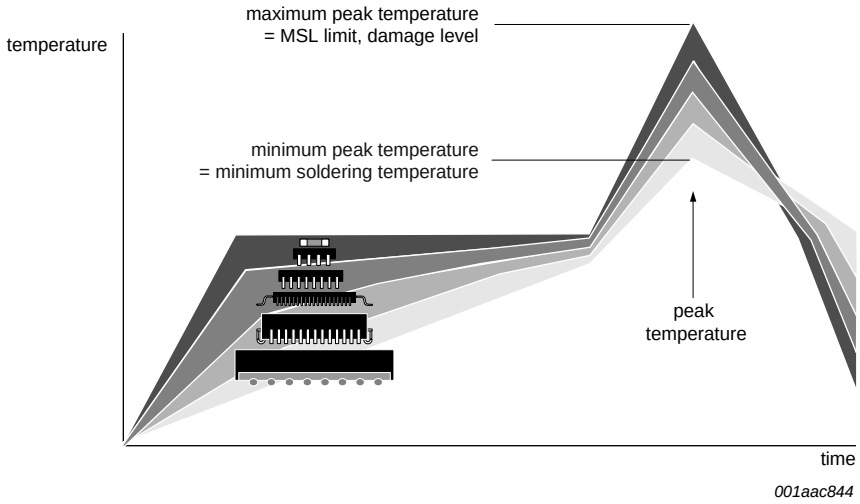
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12.

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9890_SDS v.1	20130517	Preliminary data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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