

# REALTEK

**ALC885-GR**  
**ALC885M-GR**

## **7.1+2 CHANNEL HIGH-PERFORMANCE HDA CODEC WITH CONTENT PROTECTION**

### **DATASHEET**

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**USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek ALC885 Audio Codec ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

**REVISION HISTORY**

Revision	Release Date	Summary
1.0	2006/06/06	First release.
1.1	2006/10/18	MIDI function is not supported as pins 47 and 48 are assigned as S/PDIF IO

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## 1. General Description

The ALC885 is a high-performance 7.1+2 Channel High Definition Audio Codec with advanced lossless content protection technology that protects pre-recorded content while still allowing full-rate audio enjoyment from DVD audio, Blu-ray DVD, or HD DVD discs.

The ALC885 provides ten DAC channels that simultaneously support 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel stereo outputs. Three stereo ADCs are integrated and can support a microphone array with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies simultaneously.

All analog IO are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched depending on the connected device type.

Support for 16/20/24-bit S/PDIF input and output offers easy connection of PCs to high-quality consumer electronic products such as digital decoders and speakers. The series incorporates Realtek proprietary converter technology to achieve 106dB Signal-to-Noise ratio (SNR) playback quality and 101dB SNR recording quality, and is designed for Windows Vista premium desktop and laptop systems.

The ALC885 supports host/soft audio from the Intel ICH series chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like Karaoke mode, environment emulation, software equalizer, HRTF 3D positional audio, and optional Dolby® Master Studio™, the ALC885 provides an excellent home entertainment package and game experience for PC users.

## 2. Features

### 2.1. *Hardware Features*

- High-performance DACs with 106dB dynamic range (A-Weight), ADCs with 101dB dynamic range (A-Weight)
- Meets performance requirements for Microsoft WLP 3.0 Premium desktop and mobile PCs
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of concurrent independent stereo sound output (multiple streaming) through the front panel output
- There stereo ADCs support 16/20/24-bit PCM format, one for stereo microphone, one for legacy mixer recording
- All DACs and ADCs supports 44.1k/48k/96k/192kHz sample rate
- 16/20/24-bit S/PDIF-OUT supports 44.1k/48k/96k/192kHz sample rate
- 16/20/24-bit S/PDIF-IN supports 44.1k/48k/96k/192kHz sample rate
- Supports 444.1k/48k/96k/192kHz ADAT® digital output
- Up to four channels of microphone array input are supported for AEC/BF application
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.75V VREFOUT
- Two jack detection pins each designed to detect up to 4 jacks
- Supports legacy analog mixer architecture
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for each re-tasking jack
- Two GPIOs (General Purpose Input and Output) for customized applications, and digital GPI Volume Control
- Supports anti-pop mode when analog power AVDD is on and digital power is off.
- Supports stereo digital microphone interface for improved voice quality
- Content Protection for Full Rate lossless Audio content playback (with selected versions of WinDVD/PowerDVD)
- 48-pin LQFP ‘Green’ package

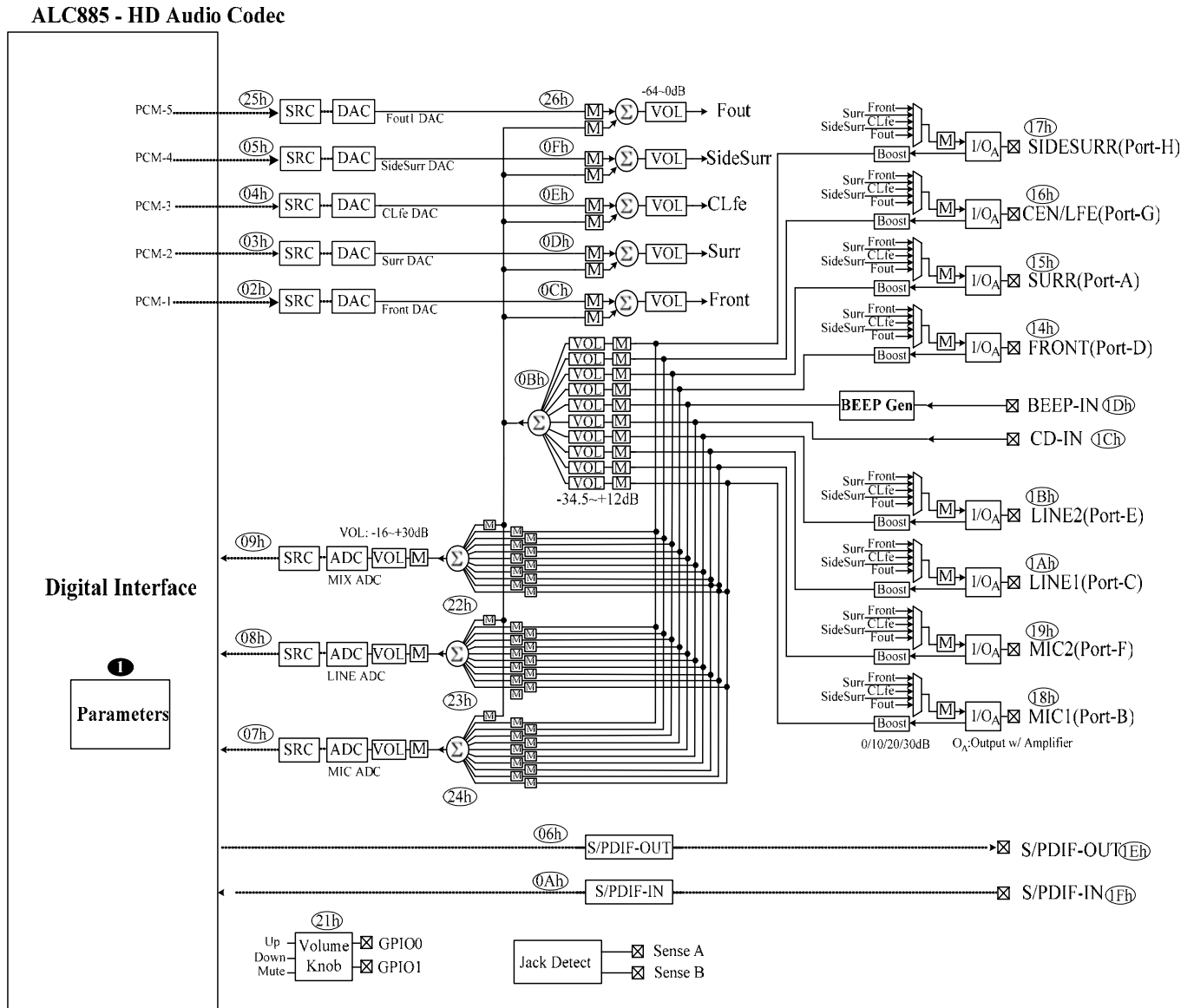
## ***2.2. Software Features***

- Compatible with Windows Vista Premium (complies with Microsoft WLP 3.0 specifications)
- WaveRT-based audio function driver for Windows Vista
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio
- 7.1+2 channel multi-streaming enables concurrent gaming/VoIP
- Friendly user interface for 2-foot or 10-foot remote control applications
- Emulation of 26 sound environments to enhance gaming experience
- 10-Band Software Equalizer
- Voice Cancellation and Key Shifting in Karaoke mode
- Realtek Media Player
- Enhanced Configuration Panel to improve user experience
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- ALC885M-GR features Dolby® Master Studio™ (optional software feature)

## **3. System Applications**

- Desktop multimedia PCs
- Laptop PCs
- Information appliances (IA) e.g., set-top box

## 4. Block Diagram



**Figure 1. Block Diagram**

## 4.1. Analog Input/Output Unit

Pin Complex widgets NID=14h~1Bh are re-tasking IOs.

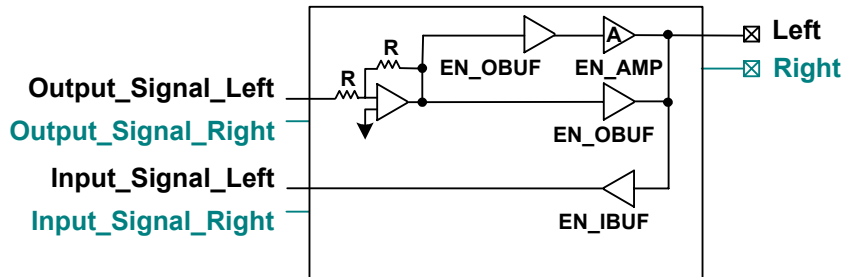


Figure 2. Analog Input/Output Unit

## 5. Pin Assignments

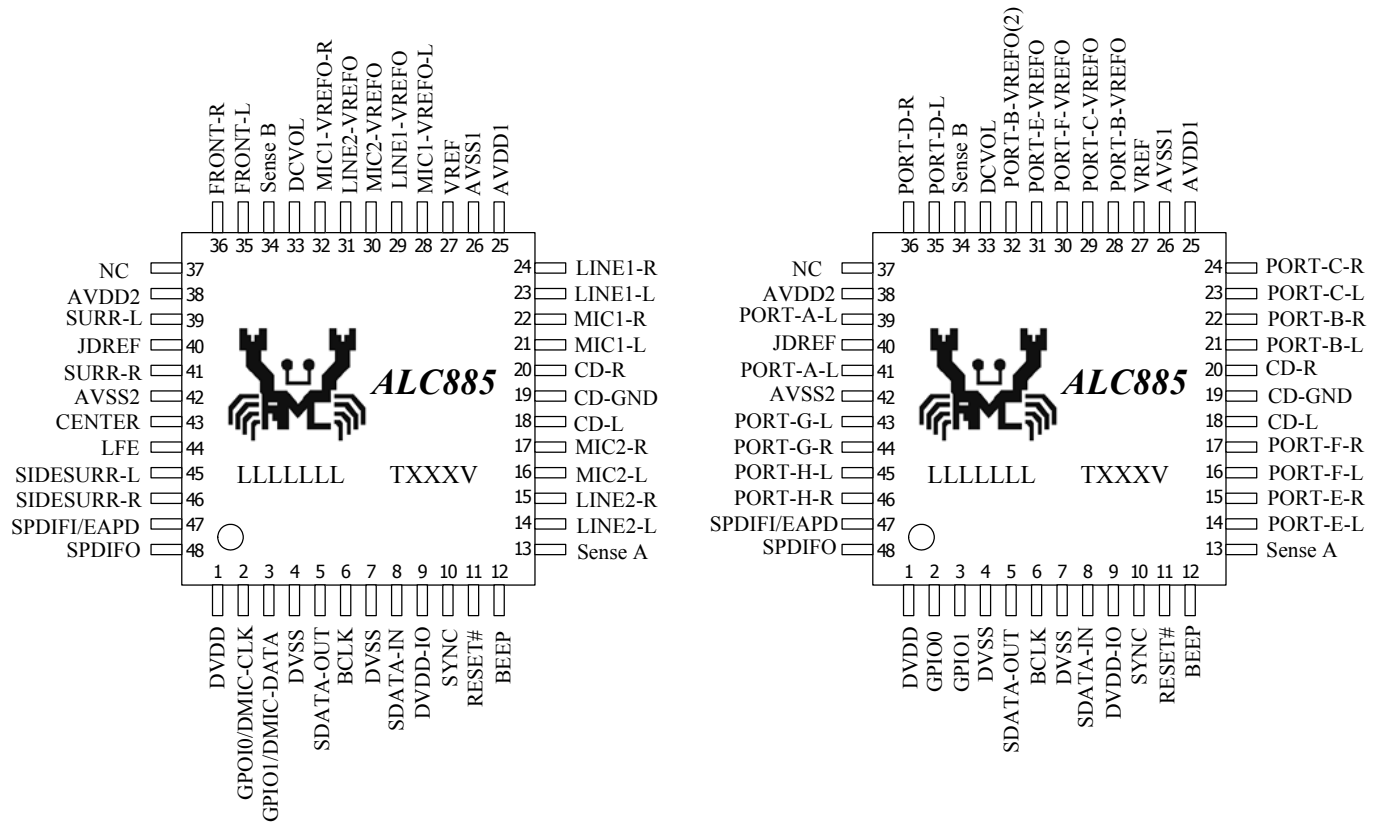


Figure 3. Pin Assignments

### 5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'V'.

## 6. Pin Descriptions

### 6.1. Digital I/O Pins

**Table 1. Digital I/O Pins**

Name	Type	Pin	Description	Characteristic Definition
RESET#	I	11	H/W reset	$V_i=0.5*DVDD$
SYNC	I	10	Sample Sync (48kHz)	$V_i=0.5*DVDD$
BITCLK	I	6	24MHz Bit clock input	$V_i=0.5*DVDD$
SDATA-OUT	I	5	Serial TDM data input	$V_i=0.5*DVDDIO$
SDATA-IN	O	8	Serial TDM data output	$V_i=0.5*DVDDIO, V_{OH}=DVDDIO, V_{OL}=DVSS$
SPDIF-IN/ EAPD* <sup>1</sup>	I/O	47	Digital S/PDIF Input / Signal to power down ext. amp /	$V_{IL}=1.45V, V_{IH}=1.85V /$ $V_{OH}=DVDD, V_{OL}=DVSS$
SPDIF-OUT* <sup>2</sup>	O	48	Digital S/PDIF output and ADAT Output	Output has 12mA@75Ω driving capability $V_{OH}=DVDD, V_{OL}=DVSS$
GPIO0 / DMIC-CLK	I/O	2	General Purpose Input/Output 0 Clock output to digital MIC	Input: $V_t=(2/3)*DVDD$ Output: $V_{OH}=DVDD, V_{OL}=DVSS$
GPIO1 / DMIC-DATA	I/O	3	General Purpose Input/Output 1 Serial data in from digital MIC	Input: $V_t=(2/3)*DVDD$ Output: $V_{OH}=DVDD, V_{OL}=DVSS$
				Total: 9 Pins

\*<sup>1</sup>: Pin 47 can be configured to support secondary digital mic input (DMIC-R). It is supported via a customized Realtek driver

\*<sup>2</sup>: Pin 48 can output ADAT digital audio output. The function is enabled via a customized Realtek driver.

### 6.2. Analog I/O Pins

**Table 2. Analog I/O Pins**

Name	Type	Pin	Description	Characteristic Definition
LINE2-L	IO	14	2 <sup>nd</sup> line input left channel	Analog input/output, default is input (JACK-E)
LINE2-R	IO	15	2 <sup>nd</sup> line input right channel	Analog input/output, default is input (JACK -E)
MIC2-L	IO	16	2 <sup>nd</sup> stereo microphone input left channel	Analog input/output, default is input (JACK -F)
MIC2-R	IO	17	2 <sup>nd</sup> stereo microphone input right channel	Analog input/output, default is input (JACK -F)
CD-L	I	18	CD input left channel	Analog input, 1.6Vrms of full scale input
CD-G	I	19	CD input reference ground	Analog input, 1.6Vrms of full scale input
CD-R	I	20	CD input right channel	Analog input, 1.6Vrms of full scale input
MIC1-L	IO	21	1 <sup>st</sup> stereo microphone input left channel	Analog input/output, default is input (JACK -B)
MIC1-R	IO	22	1 <sup>st</sup> stereo microphone input right channel	Analog input/output, default is input (JACK -B)
LINE1-L	IO	23	1 <sup>st</sup> line input left channel	Analog input/output, default is input (JACK -C)
LINE1-R	IO	24	1 <sup>st</sup> line input right channel	Analog input/output, default is input (JACK -C)

Name	Type	Pin	Description	Characteristic Definition
PCBEEP	I	12	External PCBEEP input	Analog input, 1.6Vrms of full scale input
FRONT-L	IO	35	Front output left channel	Analog output (JACK -D)
FRONT-R	IO	36	Front output right channel	Analog output (JACK -D)
SURR -L	IO	39	Surround out left channel	Analog output (JACK -A)
SURR -R	IO	41	Surround out right channel	Analog output (JACK -A)
CENTER	O	43	Center output	Analog output (JACK -G)
LFE	O	44	Low Frequency output	Analog output (JACK -G)
SIDESURR -L	O	45	Side output left channel	Analog output (JACK -H)
SIDESURR -R	O	46	Side output right channel	Analog output (JACK -H)
Sense A	I	13	Jack Detect pin 1	Jack resistor network input 1
Sense B	I	34	Jack Detect pin 2	Jack resistor network input 2
				Total: 22 Pins

### 6.3. Filter/Reference/NC

**Table 3. Filter/Reference**

Name	Type	Pin	Description	Characteristic Definition
VREF	-	27	2.5V Reference voltage	10uf capacitor to analog ground
MIC1-VREFO-L	O	28	Bias voltage for MIC1 jack	2.5V/3.75V reference voltage
LINE1-VREFO	O	29	Bias voltage for LINE1 jack	2.5V/3.75V reference voltage
MIC2-VREFO	O	30	Bias voltage for MIC2 jack	2.5V/3.75V reference voltage
LINE2-VREFO	O	31	Bias voltage for LINE2 jack	2.5V/3.75V reference voltage
MIC1-VREFO-R	O	32	Bias voltage for MIC1 jack	2.5V/3.75V reference voltage
NC	-	37	Not Connected	
JDREF	-	40	Reference resistor for Jack detection	20K, 1% external resistor to analog ground
				Total: 8 Pins

### 6.4. Power/Ground

**Table 4. Power/Ground**

Name	Type	Pin	Description	Characteristic Definition
AVDD1	I	25	Analog VDD	Analog power for mixer and amplifier
AVSS1	I	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	I	38	Analog VDD	Analog power for DACs and ADCs
AVSS2	I	42	Analog GND	Analog ground for DACs and ADCs
DVDD	I	1	Digital VDD	Digital power for core
DVSS	I	4	Digital GND	Digital ground for core
DVDD-IO	I	9	Digital VDD	Digital IO power for HDA bus (1.5V~3.3V)
DVSS	I	7	Digital GND	Digital ground for HDA bus
				Total: 8 Pins



## 7. High Definition Audio Link Protocol

### 7.1. Link Signals

The High Definition Audio (HDA) link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

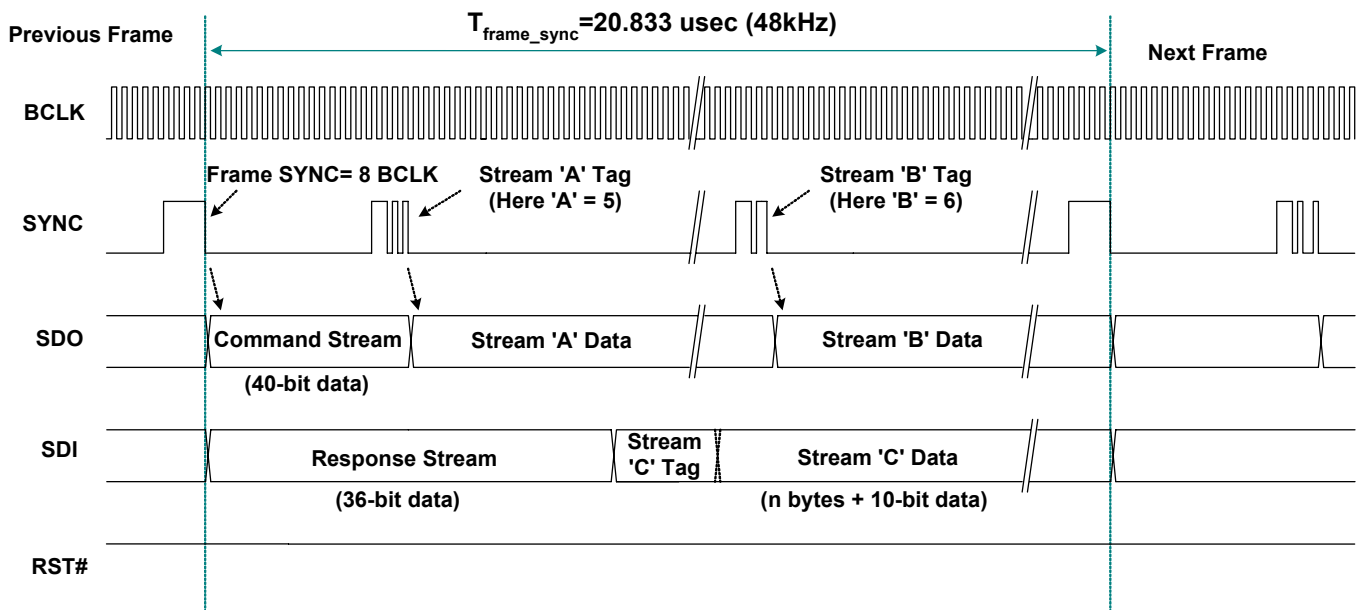


Figure 4. HDA Link Protocol

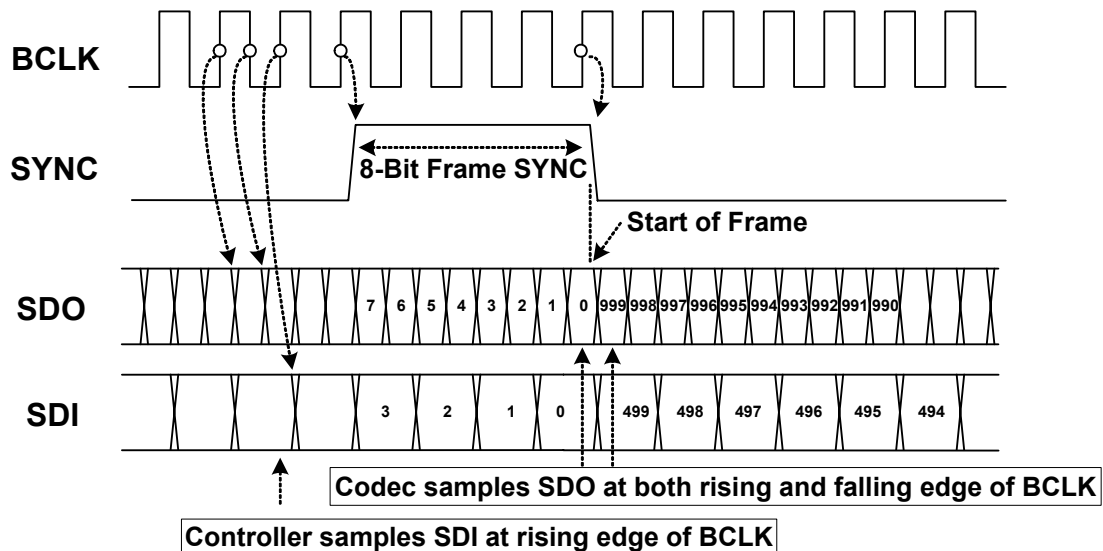
### 7.1.1. Signal Definitions

**Table 5. Link Signal Definitions**

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connecting to all codecs
SYNC	48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs
SDO	Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported
SDI	Serial data input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs

**Table 6. HDA Signal Definitions**

Signal Name	Source	Type for Controller	Description
BCLK	Controller	Output	Global 24.0MHz bit clock
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal
SDO	Controller	Output	Serial data output from the controller
SDI	Codec/Controller	Input/Output	Serial data input from codec. Weakly pulled down by the controller
RST#	Controller	Output	Global active low reset signal


**Figure 5. Bit Timing**

### 7.1.2. Signaling Topology

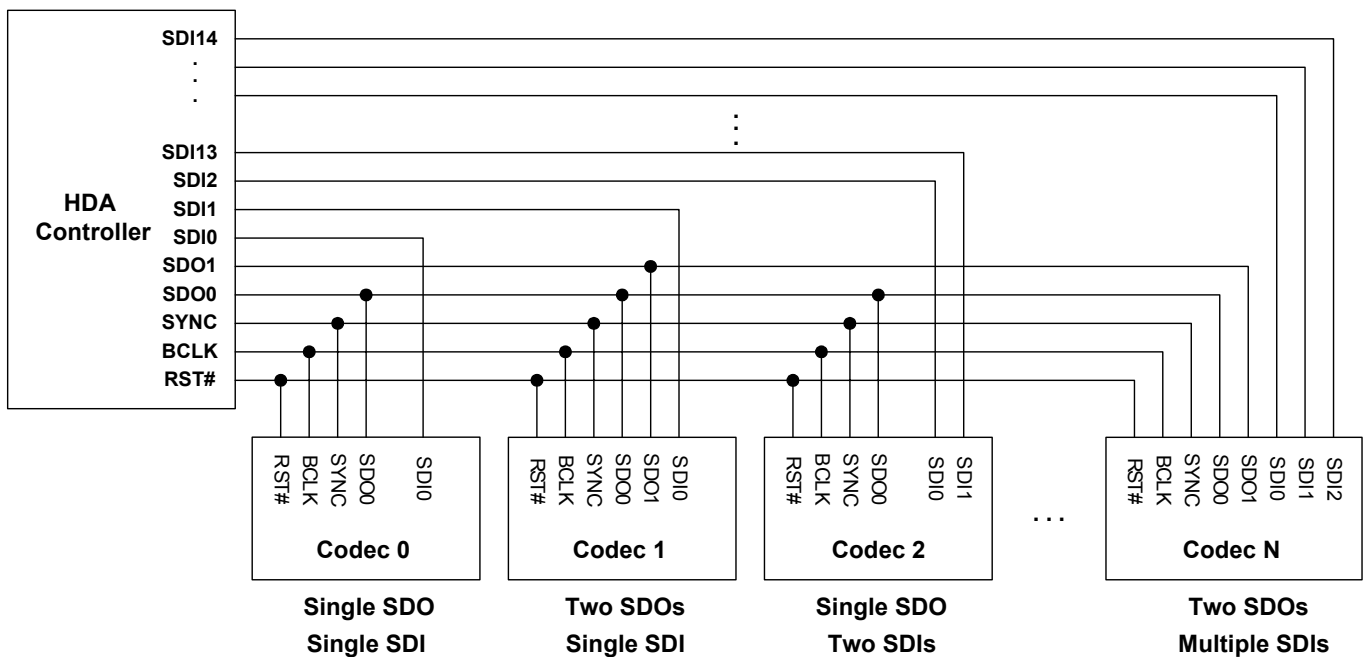
The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0, and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 12 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC885 is designed to receive a single SDO stream.



**Figure 6. Signaling Topology**

## 7.2. Frame Composition

### 7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be two blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

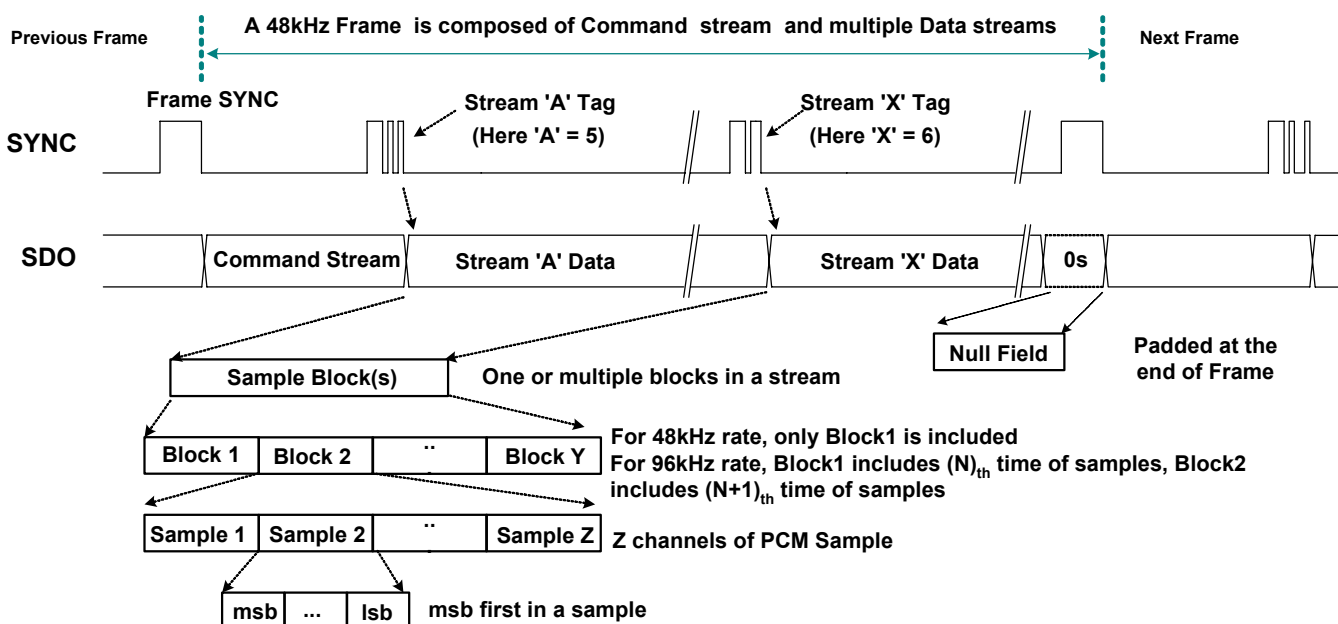


Figure 7. SDO Outbound Frame

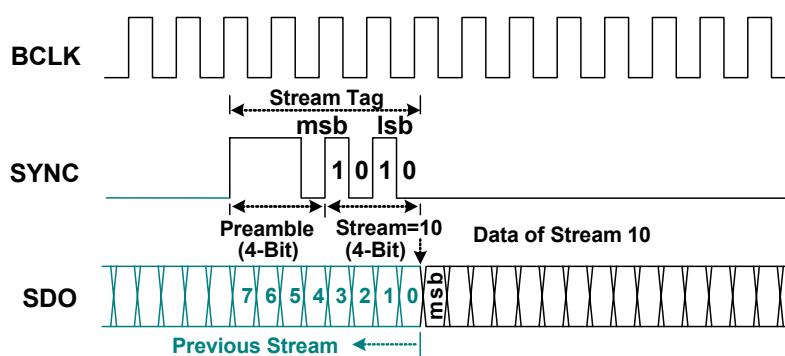


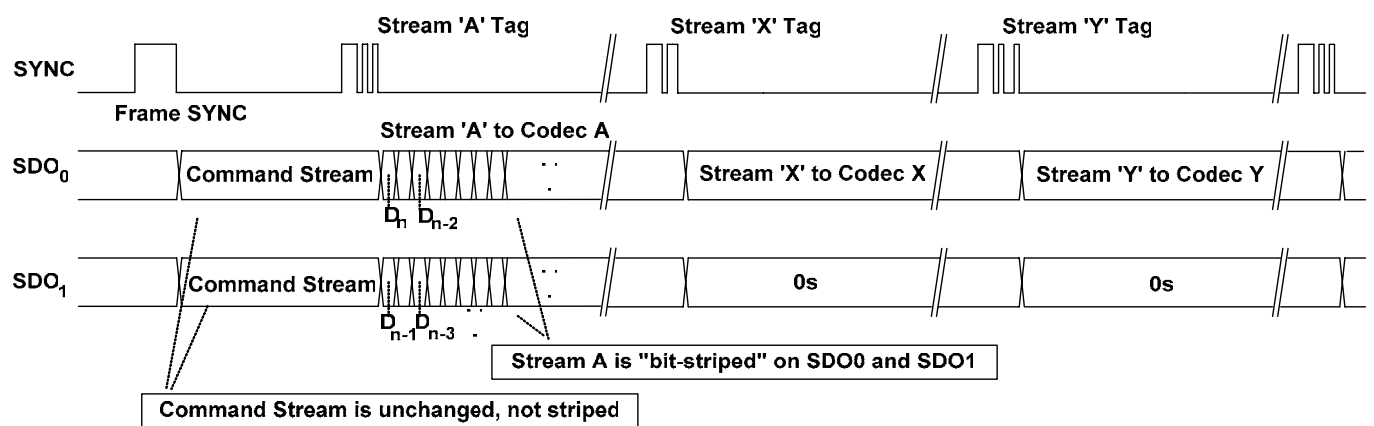
Figure 8. SDO Stream Tag is Indicated in SYNC

### 7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the ‘Stripe Control’ bit in the controller’s Output Stream Control Register to initiate a specific stream (Stream ‘A’ in Figure 9) to be transmitted on multiple SDOs. In this case, the MSB of the data stream is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.



**Figure 9. Striped Stream on Multiple SDOs**

### 7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), the SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 10).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 11).

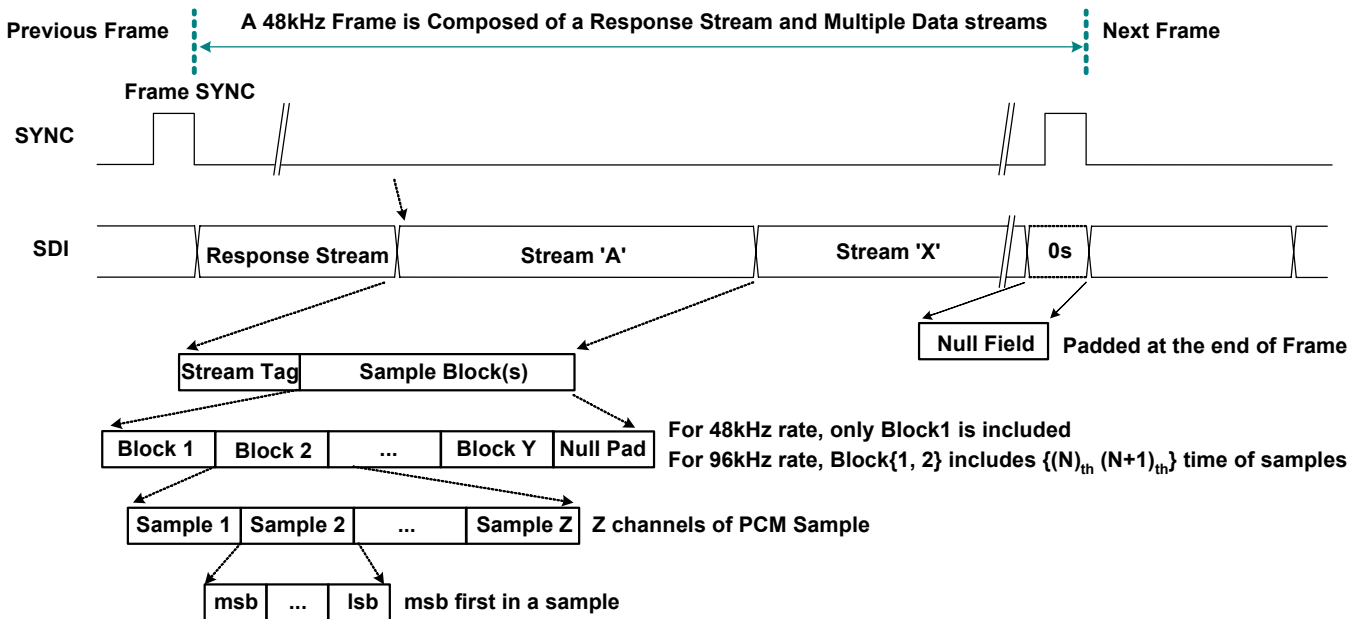


Figure 10. SDI Inbound Stream

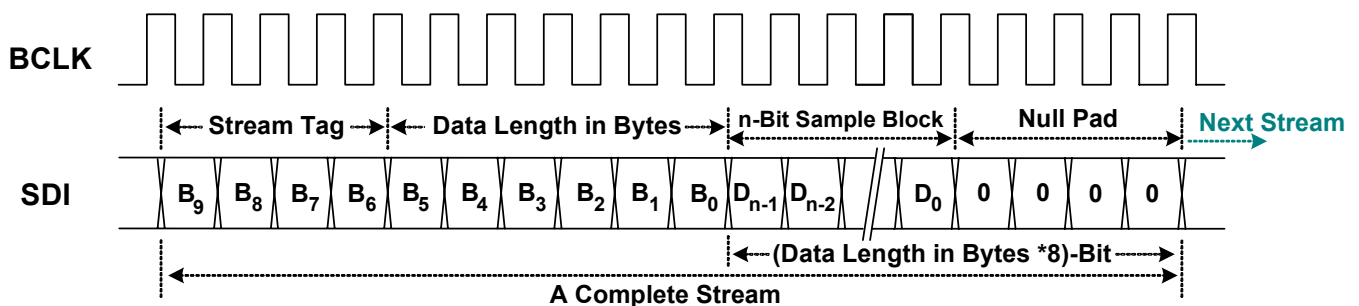
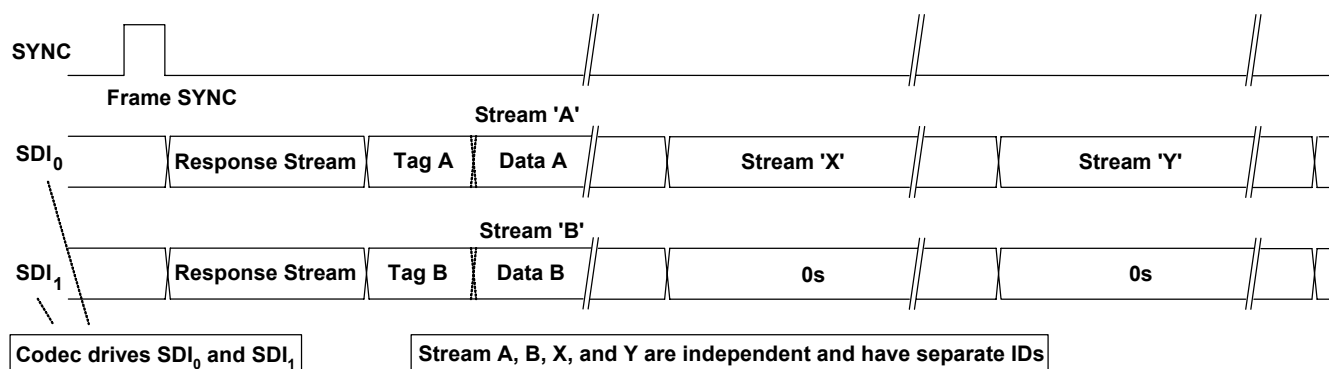


Figure 11. SDI Stream Tag and Data

### 7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data into separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.



**Figure 12. Codec Transmits Data Over Multiple SDIs**

### 7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 16, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 16, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames. The cadence “12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)” interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain

n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 9, page 17).

**Table 7. Defined Sample Rate and Transmission Rate**

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	
1/2		22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

**Table 8. 48kHz Variable Rate of Delivery Timing**

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y <sup>2</sup> NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y <sup>2</sup> (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y <sup>4</sup> (repeat)	Four sample blocks are transmitted in each frame

*N: No sample block in a frame*

*Y: One sample block in a frame*

*Y<sup>x</sup>: X sample blocks in a frame*





### ***7.3. Reset and Initialization***

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset
2. Codec Reset
3. Codec changes its power state (for example, hot docking a codec to an HDA system)

#### **7.3.1. Link Reset**

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the ‘CRST’ bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 13, page 19, shows the ‘Link Reset’ timing including the ‘Enter’ sequence (❶~❺) and ‘Exit’ sequence (❻~❾)

Enter ‘Link Reset’:

- ❶ Software writes a 0 to the ‘CRST’ bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ When the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RST# signal to low, and enters the ‘Link Reset’ state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

- ⑥ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)
- ⑦ Software is responsible for de-asserting RST# after a minimum of 100 $\mu$ s BCLK running time (the 100 $\mu$ sec provides time for the codec PLL to stabilize)
- ⑧ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC
- ⑨ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

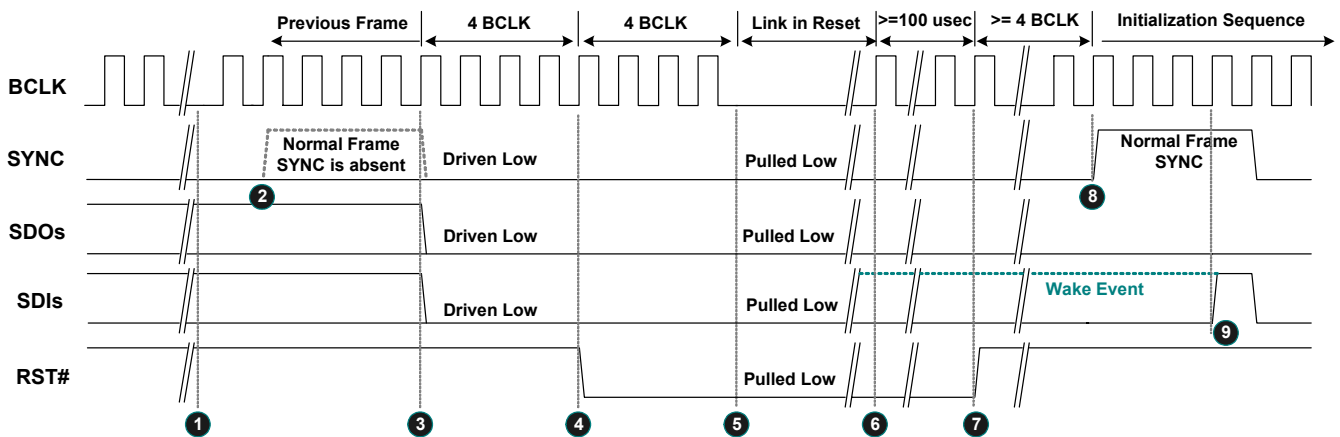


Figure 13. Link Reset Timing

### 7.3.2. Codec Reset

A 'Codec Reset' is initiated via the codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

### 7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec will stop driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operation state

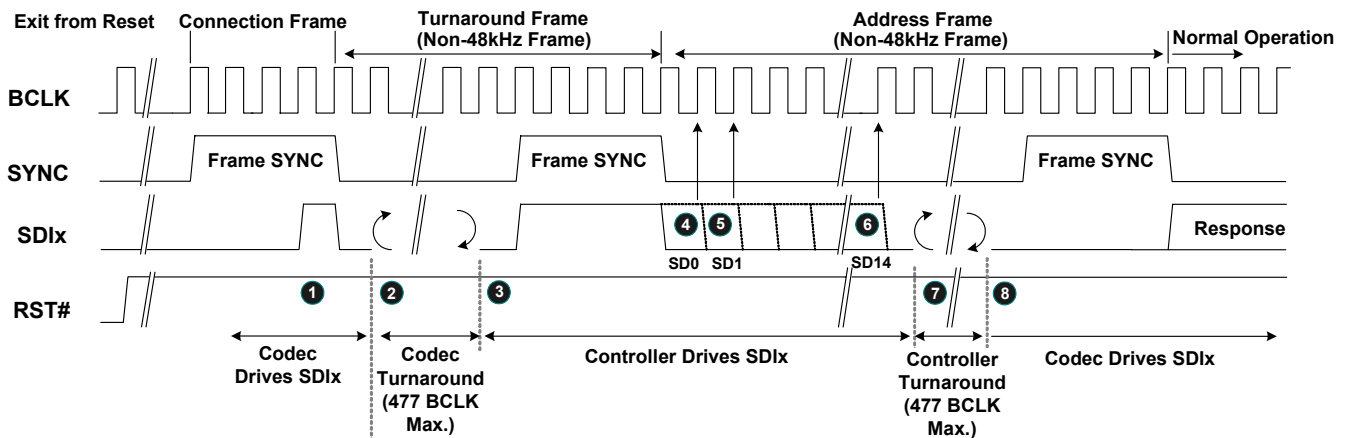


Figure 14. Codec Initialization Sequence

## ***7.4. Verb and Response Format***

### **7.4.1. Command Verb Format**

There are two types of verbs; one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 10 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-bit verb structure that gets and controls parameters in the codec.

**Table 10. 40-Bit Commands in 4-Bit Verb Format**

<b>Bit [39:32]</b>	<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Bit [15:0]</b>
Reserved	Codec Address	Node ID	Verb ID	Payload

**Table 11. 40-Bit Commands in 12-Bit Verb Format**

<b>Bit [39:32]</b>	<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Bit [7:0]</b>
Reserved	Codec Address	Node ID	Verb ID	Payload

**Table 12. Verbs Supported by the ALC885 (Y=Supported)**

Supported Verb	Get Verb	Set Verb	Root Node	Audio Function Group	Modem Function Group	HDMI Function Group	Vendor Define Group	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget*1	Volume Knob	Beep Generator	Vendor Defined Widget
Get parameter	F00		Y	Y				Y	Y	Y	Y	Y	Y	Y	Y	Y
Connection Select	F01	701							Y	Y		Y				
Get Connection List Entry	F02								Y	Y	Y	Y				
Processing State	F03	703														
Coefficient Index	D-	5-														Y
Processing Coefficient	C-	4-														Y
Amplifier Gain/Mute	B-	3-							Y	Y	Y					
Stream Format	A-	2-						Y	Y							
Digital Converter 1	F0D	70D						Y	Y							
Digital Converter 2	F0D	70E						Y	Y							
Power State	F05	705		Y												
Channel / Stream ID	F06	706						Y	Y							
SDI Select	F04	704														
Pin Widget Control	F07	707								Y						
Unsolicited Enable	F08	708								Y				Y		
Pin Sense	F09	709								Y						
EAPD / BTL Enable	F0C	70C														
All GPIO Control	F10 - F1A	710 - 71A		Y												
Beep Generator Control	F0A	70A													Y	
Volume Knob Control	F0F	70F												Y		
Subsystem ID, Byte 0	F20	720		Y												
Subsystem ID, Byte 1	F20	721		Y												
Subsystem ID, Byte 2	F20	722		Y												
Subsystem ID, Byte 3	F20	723		Y												
Config Default, Byte 0	F1C	71C								Y						
Config Default, Byte 1	F1C	71D								Y						
Config Default, Byte 2	F1C	71E								Y						
Config Default, Byte 3	F1C	71F								Y						
RESET		7FF		Y												

**Table 13. Parameters in the ALC885 (Y=Supported)**

Supported Parameter	Parameter ID	Root Node	Audio Function Group	Modem Function Group	HDMI Function Group	Vendor Define Group	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget <sup>*1</sup>	Volume Knob	Beep Generator	Vendor Defined Widget
Vendor ID	00	Y													
Revision ID	02	Y													
Subordinate Node Count	04	Y	Y												
Function Group Type	05		Y												
Audio Function Group Capabilities	08		Y												
Audio Widget Capabilities	09						Y	Y	Y	Y	Y	Y	Y	Y	Y
Sample Size, Rate	0A		Y				Y	Y							
Stream Formats	0B		Y				Y	Y							
Pin Capabilities	0C								Y						
Input Amp Capabilities	0D							Y		Y	Y				
Output Amp Capabilities	12								Y	Y					
Connection List Length	0E							Y	Y	Y	Y				
Supported Power States	0F		Y				Y	Y	Y	Y	Y				Y
Processing Capabilities	10														Y
GPI/O Count	11		Y												
Volume Knob Capabilities	13												Y		

## 7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The ‘Tag’ in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

**Table 14. Solicited Response Format**

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

**Table 15. Unsolicited Response Format**

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

*Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a ‘Valid’ bit to indicate the response is ‘Ready’. Bit-34 is set to indicate that an unsolicited response was sent.*

## 7.5. Power Management

The ALC885 does not support Wake-Up events when in low power mode. All power management state changes in widgets are driven by software. Table 16 shows the System Power State Definitions.

In the ALC885, all the widgets, including output/input converters, support power control. Software may have various power states depending on system configuration.

Table 17 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-grained power control.

**Table 16. System Power State Definitions**

Power States	Definitions
D0	All power on. Individual DACs and ADCs can be powered up or down as required
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference is off (D1 + analog reference off)
D3 (Hot)	Power still supplied. The codec stops the internal clock. State is maintained
D3 (Cold)	All power removed. State lost



**Table 17. Power Controls in NID 01h**

Item	Description	D0	D1	D2	D3	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	FRONT DAC (NID 02h)	Normal	PD	PD	PD	PD
	SURR DAC (NID 03h)	Normal	PD	PD	PD	PD
	CEN/LFE DAC (NID 04h)	Normal	PD	PD	PD	PD
	SIDESURR DAC (NID 05h)	Normal	PD	PD	PD	PD
	FOUT DAC (NID 25h)	Normal	PD	PD	PD	PD
	MIC ADC (NID07h)	Normal	PD	PD	PD	PD
	LINE ADC (NID08h)	Normal	PD	PD	PD	PD
	MIX ADC (NID 09h)	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down

**Table 18. Powered Down Conditions**

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. S/PDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied
FRONT DAC powered down	Analog block and digital filter are powered down
SURR DAC powered down	Analog block and digital filter are powered down
CEN/LFE DAC powered down	Analog block and digital filter are powered down
SIDESURR DAC powered down	Analog block and digital filter are powered down
FOUT DAC powered down	Analog block and digital filter are powered down
LINE ADC powered down	Analog block and digital filter are powered down. Data on SDATA-IN is quiet
MIX ADC powered down	Analog block and digital filter are powered down. Data on SDATA-IN is quiet
MIC ADC powered down	Analog block and digital filter are powered down. Data on SDATA-IN is quiet
Headphone Driver powered down	All headphone drivers are powered down
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off

## 8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC885. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

### 8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget. Some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, page 21, for detailed information about supported parameters.

**Table 19. Verb – Get Parameters (Verb ID=F00h)**

Get Parameter Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]	32-bit Response

*Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.*

#### 8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

**Table 20. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)**

Codec Response Format	
Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID)
15:0	Device ID=0885h

*Note: The Root Node (NID=00h) supports this parameter.*

#### 8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

**Table 21. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)**

Codec Response Format	
Bit	Description
31:24	Reserved. Read as 0's
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC885 is fully compliant. Response=0x1
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC885 is fully compliant. Response=0x0
15:8	Revision ID. The vendor's revision number 00h is for the first silicon version (A version), 01h is for the second version (B version), etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID

*Note: The Root Node (NID=00h in the ALC885) supports this parameter.*

### 8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

**Table 22. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)**

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:16	Starting Node Number The starting node number in the sequential widgets
15:8	Reserved. Read as 0's
7:0	Total Number of Nodes For a root node, the total number of function groups in the root node For a function group, the total number of widget nodes in the function group

	Description	Reserved	Starting Node	Reserved	Total Fun/Widgets
	Bits →	Bit [31:24]	Bit [23:16]	Bit [15:8]	Bit [7:0]
Root Node	NID=00h	-	01h	-	01h
Audio Function	NID=01h	-	02h	-	25h
Others		Not supported (returns 00000000h)			

### 8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

**Table 23. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)**

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's
8	UnSol Capable. Read as 1. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type. Read as 01h. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function

*Note: The Audio Function Group (NID=01h) supports this parameter.*

### 8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

**Table 24. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)**

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's
16	Beep Generator, read as 1. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group
15:12	Reserved. Read as 0's
11:8	Input Delay. Read as 0xF.
7:4	Reserved. Read as 0's
3:0	Output Delay. Read as 0xF.

Note: The Audio Function Group (NID=01h) supports this parameter.

### 8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

**Table 25. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)**

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:20	Widget Type 0h: Audio Output    1h: Audio Input    2h: Mixer    3h: Selector    4h: Pin Complex 5h: Power Widget    6h: Volume Knob Widget    7h~Eh: Reserved    Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets
15:11	Reserved. Read as 0's
10	Power Control 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0
4	Format Override

**Codec Response Format**

Bit	Description
3	AmpParOvr, AMP Param Override
2	OutAmpPre. Out AMP Present
1	InAmpPre. In AMP Present
0	Stereo 0: Mono Widget 1: Stereo Widget

**Table 26. Widget Capability Support**

		Reserved								Widget Type				Delay				Reserved				Power Control	Digital	ConnList	UnsolCap	ProcWidget	Reserved	Format Override	AmpParOvr	OutAmpPre	InAmpPre	Stereo					
	Bits →	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0				
Root Node	NID=00h	Not supported (returns 00000000h)																																			
Audio Function	NID=01h	Not supported (returns 00000000h)																																			
Output Converters	NID=02h	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	1	0	0	0	0	0	1				
	NID=03h	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	1	0	0	0	0	0	1				
	NID=04h	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	1	0	0	0	0	0	1				
	NID=05h	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	1	0	0	0	0	0	1				
	NID=25h	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	1	0	0	0	0	0	1				
	NID=06h (S/PDIF-OUT)	-	-	-	-	-	-	-	-	0h	0	-	0	0	0	1	0	0	0	0	0	-	1	0	0	0	0	0	0	0	0	0	1				
Input Converters	NID=07h	-	-	-	-	-	-	-	-	1h	0	-	0	0	0	0	1	0	0	0	0	-	1	1	0	1	1	0	1	1	1	1	1				
	NID=08h	-	-	-	-	-	-	-	-	1h	0	-	0	0	0	0	1	0	0	0	0	-	1	1	0	1	1	0	1	1	1	1	1				
	NID=09h	-	-	-	-	-	-	-	-	1h	0	-	0	0	0	0	1	0	0	0	0	-	1	1	0	1	1	0	1	1	1	1	1				
	NID=0Ah (S/PDIF-IN)	-	-	-	-	-	-	-	-	1h	0	-	0	0	0	1	1	1	0	-	1	0	0	0	0	0	1	0	0	0	1	1	1				
Mixer (Sum)	NID=0Bh	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	0	1	0	1	1	0	1	1	1	1	1				
	NID=0Ch	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	1	1	1	1	1	0	1	1	1	1	1				
	NID=0Dh	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	1	1	1	1	1	0	1	1	1	1	1				
	NID=0Eh	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	1	1	1	1	1	0	1	1	1	1	1				
	NID=26h	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	1	1	1	1	1	0	1	1	1	1	1				
	NID=0Fh	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	1	1	1	1	1	0	1	1	1	1	1				
	NID=22h	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	0	1	0	1	1	0	1	1	1	1	1				
	NID=23h	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	0	1	0	1	1	0	1	1	1	1	1				
	NID=24h	-	-	-	-	-	-	-	-	2h	0	-	0	0	0	0	1	0	0	-	0	1	0	1	0	1	1	0	1	1	1	1	1				

	Bits →	Reserved								Widget Type				Delay				Reserved				Power Control	Digital	ConnList	UnsolCap	ProcWidget	Reserved	Format Override	AmpParOvr	OutAmpPre	InAmpPre	Stereo	
		3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
Pin Complex	NID=14h (FRONT)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=15h (SURR)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=16h (CEN/LF E)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=17h (SIDESU RR)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=18h (MIC1)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=19h (MIC2)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=1Ah (LINE1)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=1Bh (LINE2)	-								4h				0				-				0	0	0	1	1	0	-	0	1	1	1	1
	NID=1Ch (CD-IN)	-								4h				0				-				0	0	0	0	0	0	-	0	0	0	0	1
	NID=1Dh (BEEP)	-								4h				0				-				0	0	0	0	0	0	-	0	0	0	0	0
	NID=1Eh (S/PDIF- OUT)	-								4h				0				-				0	0	1	1	0	0	-	0	0	0	0	0
NID=1Fh (S/PDIF- IN)	-								4h				0				-				0	0	1	0	0	0	-	0	0	0	0	0	
Vol- ume Knob	NID=21h	-								6h				-				-				0	0	0	0	1	0	-	0	0	0	0	0
Vendor Define	NID=20h	-								Fh				-				-				0	0	0	0	0	1	-	0	0	0	0	0
	NID=10h ~13h	-								Fh				-				-				0	0	0	0	0	0	-	0	0	0	0	0

### 8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameters here provide default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

**Table 27. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)**

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's
20	B32. 32-bit audio format support 0: Not supported 1: Supported
19	B24. 24-bit audio format support 0: Not supported 1: Supported
18	B20. 20-bit audio format support 0: Not supported 1: Supported
17	B16. 16-bit audio format support 0: Not supported 1: Supported
16	B8. 24-bit audio format support 0: Not supported 1: Supported
15:12	Reserved. Read as 0's
11	R12. 384kHz (=8*48kHz) rate support 0: Not supported 1: Supported
10	R11. 192kHz (=4*48kHz) rate support 0: Not supported 1: Supported
9	R10. 176.4kHz (=4*44.1kHz) rate support 0: Not supported 1: Supported
8	R9. 96kHz (=2*48kHz) rate support 0: Not supported 1: Supported
7	R8. 88.2kHz (=2*44.1kHz) rate support 0: Not supported 1: Supported
6	R7. 48kHz rate support 0: Not supported 1: Supported

**Codec Response Format**

<b>Bit</b>	<b>Description</b>
5	R6. 44.1kHz rate support 0: Not supported 1: Supported
4	R5. 32kHz ( $=2/3*48\text{kHz}$ ) rate support 0: Not supported 1: Supported
3	R4. 22.05kHz ( $=1/2*44.1\text{kHz}$ ) rate support 0: Not supported 1: Supported
2	R3. 16kHz ( $=1/3*48\text{kHz}$ ) rate support 0: Not supported 1: Supported
1	R2. 11.025kHz ( $=1/4*44.1\text{kHz}$ ) rate support 0: Not supported 1: Supported
0	R1. 8kHz ( $=1/6*48\text{kHz}$ ) rate support 0: Not supported 1: Supported



**Table 28. Sample Rate and PCM Size Supported in Each Converter**

	Description	Reserved										B	B	B	B	B	Reserved				R	R	R	R	R	R	R	R	R	R	R								
		3	3	2	2	2	2	2	2	2	2	2	3	2	2	1	8	1	1	1	1	1	2	1	1	0	9	8	7	6	5	4	3	2	1				
	<b>Bits →</b>	3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0			
Audio Function	NID=01h	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	
Output Converters	NID=02h (Front DAC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	
	NID=03h (Surr DAC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=04h (Cen/Lfe DAC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=05h (SideSurr DAC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=25h (Fout DAC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=06h (S/PDIF-OUT)	-										1	1	1	1	0	-				0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Input Converters	NID=07h (MIC ADC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=08h (LINE ADC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=09h (MIX ADC)	-										0	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	NID=0Ah (S/PDIF-IN)	-										1	1	1	1	0	-				0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Others		Not supported (returns 00000000h)																																					

### 8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

**Table 29. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)**

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's
2	AC3 0: Not supported 1: Supported
1	Float32 0: Not supported 1: Supported
0	PCM 0: Not supported 1: Supported

*Note: Input converters and output converters support this parameter.*

**Table 30. Stream Format Supported in Each Converter**

Input converters and output converters support this parameter.

	Description	Reserved	AC3	Float32	PCM
	Bits →	Bit [31:3]	Bit [2]	Bit [1]	Bit [0]
Audio Function	NID=01h	-	0	0	1
Output Converters	NID=02h~06h, 25h	-	0	0	1
Input Converters	NID=07h~0Ah	-	0	0	1
Others		Not supported (returns 00000000h)			

### 8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

**Table 31. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)**

Codec Response Format

Bit	Description														
31:16	Reserved. Read as 0's														
15:8	VREF Control Capability '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD. <table border="1" data-bbox="347 591 1426 667"> <thead> <tr> <th>7:6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>100%</td> <td>80%</td> <td>Reserved</td> <td>Ground</td> <td>50%</td> <td>Hi-Z</td> </tr> </tbody> </table>	7:6	5	4	3	2	1	0	Reserved	100%	80%	Reserved	Ground	50%	Hi-Z
7:6	5	4	3	2	1	0									
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z									
7	L-R Swap. Indicates the capability of swapping the left and right														
6	Balanced I/O Pin '1' indicates this pin complex has balanced pins														
5	Input Capable '1' indicates this pin complex supports input														
4	Output Capable '1' indicates this pin complex supports output														
3	Headphone Drive Capable '1' indicates this pin complex has an amplifier to drive a headphone														
2	Presence Detect Capable '1' indicates this pin complex can detect whether there is anything plugged in														
1	Trigger Required '1' indicates whether a software trigger is required for an impedance measurement														
0	Impedance Sense Capable '1' indicates this pin complex can perform analog sense on the attached device to determine its type														

*Note: Only Pin Complex widgets support this parameter.*

**Table 32. Pin Capabilities**

	Reserved	EAPD	VREF Control Capable								L-R Swap	Balanced I/O Pins	Input Capable	Output Capable	Headphone Drive Capable	Presence Detect Capable	Trigger Required	Impedance Sense Capable	
			16	15	14	13	12	11	10	9									8
Bits →	31:17		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pin Complex	NID=14h (Front Out)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=15h (Surr Out)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=16h (Cen/Lfe Out)	0s	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
	NID=17h (SideSurr Out)	0s	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
	NID=18h (MIC1)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=19h (MIC2)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=1Ah (LINE1)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=1Bh (LINE2)	0s	0	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0
	NID=1Ch (CD-IN)	0s	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	NID=1Dh (BEEP-IN)	0s	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	NID=1Eh (S/PDIF Out)	0s	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	NID=1Fh (S/PDIF In)	0s	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Others		Not supported (returns 00000000h)																	

### 8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

**Table 33. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)**

Codec Response Format

Bit	Description
31	(Input) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. ‘0’ means the gain is fixed
7	Reserved. Read as 0
6:0	Offset Indicates which step is 0dB

**Table 34. Output Amplifier Capabilities**

		Mut Capable	Reserved										Step Size	Reserved	Number of Step									Reserved	0dB Offset								
	Bits →	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
Input Con- verters	NID=07h (MIC ADC)	1	-										0000011b (=1.0dB per step)	-	0101110b (-16.0~30dB in 47 step)									-	0010000b (=16 means 0dB)								
	NID=08h (LINE ADC)	1	-										0000011b (=1.0dB per step)	-	0101110b (-16.0~30dB in 47 step)									-	0010000b (=16 means 0dB)								
	NID=09h (MIX ADC)	1	-										0000011b (=1.0dB per step)	-	0101110b (-16.0~30dB in 47 step)									-	0010000b (=16 means 0dB)								
Mixer (Sum)	NID=0Bh	1	-										0000101b (=1.5dB per step)	-	0011111b (-34.5~12dB in 32 step)									-	0010111b (=23d means 0dB)								
	NID=0Ch	1	-										0000000b	-	0000000b									-	0000000b								

		Mut Capable	Reserved	Step Size	Reserved	Number of Step	Reserved	0dB Offset																								
Bits →	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
	NID=0Dh	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=0Eh	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=0Fh	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=26h	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=22h	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=23h	1	-	0000000b	-	0000000b	-	0000000b																								
	NID=24h	1	-	0000000b	-	0000000b	-	0000000b																								
Pin Complex	NID=14h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=15h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=16h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=17h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=18h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=19h	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=1Ah	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
	NID=1Bh	0	-	0100111b (=10dB per step)	-	0000011b (0~30dB in 4 step)	-	0000000b (=0d means 0dB)																								
Others		Not supported (returns 00000000h)																														

### 8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

**Table 35. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)**

Codec Response Format

Bit	Description
31	(Output) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. ‘0’ means the gain is fixed
7	Reserved. Read as 0
6:0	Offset. Indicates which step is 0dB

**Table 36. Input Amplifier Capabilities**

		Mute Capable	Reserved										Step Size	Reserved	Number of Step								Reserved	0dB Offset									
	Bits →	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
Mixer (Sum)	NID=0Ch	0	-										000011b (=1.0dB per step)	-	1000000b (-64~0dB in 65 step)								-	1000000b (=64 means 0dB)									
	NID=0Dh	0	-										000011b	-	1000000b								-	1000000b									
	NID=0Eh	0	-										000011b	-	1000000b								-	1000000b									
	NID=0Fh	0	-										000011b	-	1000000b								-	1000000b									
	NID=26h	0	-										000011b	-	1000000b								-	1000000b									
Pin Complex	NID=14h (FRONT)	1	-										0000000b	-	0000000b								-	0000000b									
	NID=15h (SURR)	1	-										0000000b	-	0000000b								-	0000000b									
	NID=16h (CEN/LFE)	1	-										0000000b	-	0000000b								-	0000000b									
	NID=17h (SIDESURR)	1	-										0000000b	-	0000000b								-	0000000b									
	NID=18h (MIC1)	1	-										0000000b	-	0000000b								-	0000000b									

		Mute Capable	Reserved										Step Size						Reserved	Number of Step										Reserved	0dB Offset									
	Bits →	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0							
	NID=19h (MIC2)	1	-										0000000b						-	0000000b										-	0000000b									
	NID=1Ah (LINE1)	1	-										0000000b						-	0000000b										-	0000000b									
	NID=1Bh (LINE2)	1	-										0000000b						-	0000000b										-	0000000b									
Others		Not supported (returns 00000000h)																																						

### 8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

**Table 37. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)**

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0
7	Short Form 0: Short Form 1: Long Form
6:0	Connect List Length Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (not a MUX widget)



**Table 38. Connection List Length for Widget Input Source**

		Reserved																								Short From	Connect List Length					
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8		7	6	5	4	3	2
Input Converters	NID=07h	-																								0	1					
	NID=08h	-																								0	1					
	NID=09h	-																								0	1					
	NID=0Ah	-																								0	1					
Mixer (Sum)	NID=0Bh	-																								0	A					
	NID=0Ch	-																								0	2					
	NID=0Dh	-																								0	2					
	NID=0Eh	-																								0	2					
	NID=0Fh	-																								0	2					
	NID=26h	-																								0	2					
	NID=22h	-																								0	B					
	NID=23h	-																								0	B					
Pin Complex	NID=24h	-																								0	B					
	NID=14h	-																								0	5					
	NID=15h	-																								0	5					
	NID=16h	-																								0	5					
	NID=17h	-																								0	5					
	NID=18h	-																								0	5					
	NID=19h	-																								0	5					
	NID=1Ah	-																								0	5					
	NID=1Bh	-																								0	5					
	NID=1Ch (CD-IN)	-																								0	0					
	NID=1Dh (BEEP-IN)	-																								0	0					
	NID=1Eh (S/PDIF-OUT)	-																								0	1					
NID=1Fh (S/PDIF-IN)	-																								0	0						
Others NID	Not supported (returns 00000000h)																															

### 8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

**Table 39. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)**

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's
3	D3Sup 1: Power state D3 is supported
2	D2Sup 1: Power state D2 is supported
1	D1Sup 1: Power state D1 is supported
0	D0Sup 1: Power state D0 is supported

**Table 40. Power State Supported in Each Widget**

	Description	Reserved	D3Sup	D2Sup	D1Sup	D0Sup
	Bits →	Bit [31:3]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Rood Node	NID=00h	Not supported (returns 00000000h)				
Audio Function	NID=01h	-	1	1	1	1
Output Converters	NID=02h~05h, 25h	-	0	0	0	1
	NID=06h	-	0	0	0	1
Input Converters	NID=07h~09h	-	0	0	0	1
	NID=0Ah	-	0	0	0	1
Mixer (Sum)	NID=0Bh~0Fh, 22h~24h, 26h	-	0	0	0	1
Pin Complex	NID=14h~1Fh	-	0	0	0	1
Vendor, Volume Knob	NID=20h~21h, 10h~13h	-	0	0	0	1

### 8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

**Table 41. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)**

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's
15:8	NumCoeff. Number of Coefficient
7:1	Reserved. Read as 0's
0	Benign 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

**Table 42. Coefficient Registers Supported in Realtek Defined Widget**

	Description	Reserved	NumCoeff	Reserved	Benign
	Bits →	Bit [31:3]	Bit [15:8]	Bit [7:1]	Bit [0]
Vendor Defined	NID=20h	-	11h	-	0
Others		Not supported (returns 00000000h)			

### 8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

**Table 43. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)**

Codec Response Format

Bit	Description
31	GPIWake=0 The ALC885 does not support GPIO wake up function
30	GPIUnsol=1 The ALC885 supports GPIO unsolicited response
29:24	Reserved. Read as 0's
23:16	NumGPIs=00h No GPI pin is supported
15:8	NumGPOs=00h No GPO pin is supported
7:0	NumGPIOs=02h Three GPIO pins are supported

### 8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

**Table 44. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)**

Codec Response Format for NID=21h (Volume Control Knob)

Bit	Description
31:8	Reserved. Read as 0s
7	Delta. Read as 0 0: Software will not modify the volume in Volume Control Knob 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps The total number of steps in the range of the Volume Control Knob (NID=21h), response=0x20.

Note: The Volume Control knob (NID=21h) supports this parameter.

## 8.2. Verb – Get Connection Select Control (Verb ID=F01h)

**Table 45. Verb – Get Connection Select Control (Verb ID=F01h)**

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F01h	0's

Codec Response Format

Response [31:0]
Bit[7:0] are Connection Index

Codec Response for Analog Port-A/B/C/D/E/F/G/H (NID=14h~1Bh)

Bit	Description
31:8	0's
7:0	Connection Index current settings (Default value is 00h) 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Dh 02h: Sum Widget NID=0Eh 03h: Sum Widget NID=0Fh 04h: Sum Widget NID=26h Other: Reserved

Codec Response for Digital Pin S/PDIF-OUT (NID=1Eh)

Bit	Description
31:8	0's
7:0	Connection Index current settings (Default value is 00h) 00h: Digital Converter (S/PDIF-OUT) NID=06h Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

### 8.3. Verb – Set Connection Select (Verb ID=701h)

**Table 46. Verb – Set Connection Select (Verb ID=701h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]	0's for all nodes

### 8.4. Verb – Get Connection List Entry (Verb ID=F02h)

**Table 47. Verb – Get Connection List Entry (Verb ID=F02h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=F02h	Offset Index - N[7:0]	32-bit Response

Codec Response for NID=07h (MIC ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 24h (Sum Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=08h (LINE ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 23h (Sum Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=09h (MIX ADC)

Bit	Description
15:8	Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 22h (Sum Widget) for N=0~3 Returns 00h for N>3

**Codec Response for NID=0Ah (S/PDIF-IN Converter)**

<b>Bit</b>	<b>Description</b>
31:8	Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 1Fh (S/PDIF-IN Pin Widget) for N=0~3 Returns 00h for N>3

**Codec Response for NID=0Bh (Mixer)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N+3) Returns 1Bh (Pin Complex – LINE2) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Complex – LINE1) for N=0~3 Returns 14h (Pin Complex – FRONT) for N=4~7 Returns 00h for N>7
15:8	Connection List Entry (N+1) Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7 Returns 17h (Pin Complex – SIDESURR) for N=8~11 Returns 00h for N>11
7:0	Connection List Entry (N) Returns 18h (Pin Complex – MIC1) for N=0~3 Returns 1Ch (Pin Complex – CD) for N=4~7 Returns 16h (Pin Complex – CEN/LFE) for N=8~11 Returns 00h for N>11

**Codec Response for NID=0Ch (Front Sum)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 02h (Front DAC) for N=0~3 Returns 00h for N>3

**Codec Response for NID=0Dh (Surround Sum)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 03h (Surround DAC) for N=0~3. Returns 00h for N>3.

**Codec Response for NID=0Eh (Cen/LFE Sum)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 04h (Cen/LFE DAC) for N=0~3 Returns 00h for N>3

**Codec Response for NID=0Fh (Side-Surr Sum)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 05h (Front DAC) for N=0~3 Returns 00h for N>3

**Codec Response for NID=26h (Fout Sum)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 25h (Fout1 DAC) for N=0~3 Returns 00h for N>3

**Codec Response for NID=14h~1Bh (Port-A to port-H)**

<b>Bit</b>	<b>Description</b>
31:24	Connection List Entry (N+3) Returns 0Fh (Sum Widget NID=0Fh) for N=0~3 Returns 00h for n>3
23:16	Connection List Entry (N+2) Returns 0Eh (Sum Widget NID=0Eh) for N=0~3 Returns 00h for N>3
15:8	Connection List Entry (N+1) Returns 0Dh (Sum Widget NID=0Dh) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 0Ch (Sum Widget NID=0Ch) for N=0~3 Returns 26h (Sum Widget NID=26h) for N=4~7 Returns 00h for N>7

**Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)**

<b>Bit</b>	<b>Description</b>
31:16	Connection List Entry (N+3) and (N+2) Returns 0000h
15:8	Connection List Entry (N+1) Returns 00h
7:0	Connection List Entry (N) Returns 06h (S/PDIF-OUT converter) for N=0~3 Returns 00h for N>3



Codec Response for NID= 22h/23h/24h (Sum Widget before MIX/LINE/MIC ADCs)

Bit	Description
31:24	Connection List Entry (N+3) Returns 1Bh (Pin Complex – LINE2) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Complex – LINE1) for N=0~3 Returns 14h (Pin Complex – FRONT) for N=4~7 Returns 0Bh (Sum Widget) for N=8~11 Returns 00h for N>11
15:8	Connection List Entry (N+1) Returns 19h (Pin Complex – MIC2) for N=0~3 Returns 1Dh (Pin Complex – PCBEEP) for N=4~7 Returns 17h (Pin Complex – SIDESURR) for N=8~11 Returns 00h for N>11
7:0	Connection List Entry (N) Returns 18h (Pin Complex – MIC1) for N=0~3 Returns 1Ch (Pin Complex – CD) for N=4~7 Returns 16h (Pin Complex – CEN/LFE) for N=8~11 Returns 00h for N>11

Codec Response for Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.5. Verb – Get Processing State (Verb ID=F03h)

**Table 48. Verb – Get Processing State (Verb ID=F03h)**

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F03h	0's

Codec Response Format

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.6. Verb – Set Processing State (Verb ID=703h)

**Table 49. Verb – Set Processing State (Verb ID=703h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]	0's for all nodes

Codec Response for All NID	
<b>Bit</b>	<b>Description</b>
31:0	0's

## 8.7. Verb – Get Coefficient Index (Verb ID=Dh)

**Table 50. Verb – Get Coefficient Index (Verb ID=Dh)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=20h	Verb ID=Dh	0's	Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Defined Registers)	
<b>Bit</b>	<b>Description</b>
31:16	Reserved. Read as 0's
15:0	Coefficient Index

Codec Response for Other NID	
<b>Bit</b>	<b>Description</b>
31:0	Not supported (returns 00000000h)

## 8.8. Verb – Set Coefficient Index (Verb ID=5h)

**Table 51. Verb – Set Coefficient Index (Verb ID=5h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]	0's for all nodes

Codec Response for All NID	
<b>Bit</b>	<b>Description</b>
31:0	0's

## 8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

**Table 52. Verb – Get Processing Coefficient (Verb ID=Ch)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=20h	Verb ID=Ch	0's	Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Defined Registers)

Bit	Description
31:16	Reserved. Read as 0's
15:0	Processing Coefficient

Codec Response for Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.10. Verb – Set Processing Coefficient (Verb ID=4h)

**Table 53. Verb – Set Processing Coefficient (Verb ID=4h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]	0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

## 8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

**Table 54. Verb – Get Amplifier Gain (Verb ID=Bh)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=Bh	‘Get’ payload [15:0]	Bit[7:0] are responsible for ‘Get’

‘Get’ Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0’s
3:0	Index[3:0] for Input Source Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored

Codec Response for 07h (MIC ADC), 08h (LINE ADC) and 09h (MIX ADC)

Bit	Description
31:8	0’s
7	Bit-15 is 0 in ‘Get Amplifier Gain. Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in ‘Get Amplifier Gain. Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in ‘Get Amplifier Gain. Input Amplifier Gain [6:0]. 7-bit step value (0~46) specifying the volume from –16dB~+30dB in 1.0dB steps Bit-15 is 1 in ‘Get Amplifier Gain. Read as 0’s (No Output Amplifier Mute)

Codec Response for NID=0Bh (MIXER Sum Widget)

Bit	Description
31:8	0’s
7	Bit-15 is 0 in ‘Get Amplifier Gain. Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index) Bit-15 is 1 in ‘Get Amplifier Gain. Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in ‘Get Amplifier Gain. Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –34.5dB~+12dB in 1.5dB steps Bit-15 is 1 in ‘Get Amplifier Gain. Read as 0’s (No Output Amplifier Mute)

**Codec Response for NID=0Ch~0Fh (Sum Widget: Front, Surr, Cen/LFE, SIDESURR Sum)**

<b>Bit</b>	<b>Description</b>
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain. Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain. Read as 0 (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain. Output Amplifier Gain [6:0]. 7-bit step value (0~64) specifying the volume from -64dB~0dB in 1.0dB steps

**Codec Response for NID=14h~1Bh (Pin Complex: Front/Surr/CenLFE/SIDESURR/MIC1/MIC2/LINE1/LINE2)**

<b>Bit</b>	<b>Description</b>
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain. Read as 0 Bit-15 is 1 in 'Get Amplifier Gain. Output Amplifier Mute, 0:Unmute, 1:Mute (NID=14h~1Bh,Default=1)
6:0	Bit-15 is 0 in 'Get Amplifier Gain. Read as 0's Bit-15 is 1 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Gain)

**Codec Response to Other NID**

<b>Bit</b>	<b>Description</b>
31:0	Not supported (returns 00000000h)

## 8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

**Table 55. Verb – Set Amplifier Gain (Verb ID=3h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=3h	‘Set’ payload [7:0]	0’s for all nodes

‘Set’ Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp ‘1’ indicates output amplifier gain will be set
14	Set Input Amp ‘1’ indicates input amplifier gain will be set
13	Set Left Amp ‘1’ indicates left amplifier gain will be set
12	Set Right Amp ‘1’ indicates right amplifier gain will be set
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets) 5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the ‘Set Input Amp’ bit is not set
7	Mute 0: Unmute 1: Mute ( $-\infty$ gain)
6:0	Gain[6:0] A 7-bit step value specifying the amplifier gain

### 8.13. Verb – Get Converter Format (Verb ID=Ah)

**Table 56. Verb – Get Converter Format (Verb ID=Ah)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=Ah	0's	Bit[15:0] are converter format

Codec Response for NID=02h~06h, 25h (Output Converters: Front, Surr, Cen/LFE, Side-Surr, Fout DAC, S/PDIF-OUT).  
 Codec Response for NID=07h~0Ah (Input Converters: MIC, LINE, MIX DAC, and S/PDIF-IN)

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC885 does not support Divisor. Always read as 000b
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: reserved
3:0	Number of Channels 0: 1 channel 1: 2 channels 2: 3 channels ..... 15: 16 channels

The output converter formats supported by the ALC885 are listed. It is software's duty to set an applicable format.

	<b>BASE</b>	<b>MULT</b>	<b>DIV</b>	<b>BITS</b>	<b>Sample Rate</b>
NID=02h (Front DAC)	0	000b, 001b, 011b	000b	001, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001, 010b, 011b	44.1K
NID=03h (Surr DAC)	0	000b, 001b, 011b	000b	001, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001, 010b, 011b	44.1K
NID=04h (Cen/Lfe DAC)	0	000b, 001b, 011b	000b	001, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001, 010b, 011b	44.1K
NID=05h (Side DAC)	0	000b, 001b, 011b	000b	001, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001, 010b, 011b	44.1K
NID=25h (Fout DAC)	0	000b, 001b, 011b	000b	001, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001, 010b, 011b	44.1K
NID=06h (S/PDIF-OUT)	0	000b, 001b, 011b	000b	001, 010b, 011b, 100b	48K, 96K, 192K
	1	000b, 001b	000b	001, 010b, 011b, 100b	44.1K, 88.2K

The input converter formats supported by the ALC885 are listed. It is software's duty to set an applicable format.

	<b>BASE</b>	<b>MULT</b>	<b>DIV</b>	<b>BITS</b>	<b>Sample Rate</b>
NID=07h (MIC ADC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=08h (LINE ADC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=09h (MIX ADC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=0Ah (S/PDIF-IN)	0	000b, 001b, 011b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b, 100b	44.1K

Codec Response for other NID

<b>Bit</b>	<b>Description</b>
31:0	Not supported (returns 00000000h)



## 8.14. Verb – Set Converter Format (Verb ID=2h)

**Table 57. Verb – Set Converter Format (Verb ID=2h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:16]</b>	<b>Payload Bit [15:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID=2h	Set format [15:0]	0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1   001b: *2   010b: *3   011b: *4   100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1   001b: /2   010b: /3   011b: /4   100b: /5   101b: /6   110b: /7   111b: /8
7	Reserved. Read as 0
6:4	Bits per Sample (BITS) 000b: 8 bits   001b: 16 bits   010b: 20 bits   011b: 24 bits   100b: 32 bits   101b~111b: Reserved
3:0	Number of Channels 0: 1 channel   1: 2 channels   2: 3 channels   .....   15: 16 channels

## 8.15. Verb – Get Power State (Verb ID=F05h)

**Table 58. Verb – Get Power State (Verb ID=F05h)**

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's
5:4	PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set
3:2	Reserved. Read as 0's
1:0	PS-Set, Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.16. Verb – Set Power State (Verb ID=705h)

**Table 59. Verb – Set Power State (Verb ID=705h)**

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's
5:4	PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's
1:0	PS-Set. Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

## 8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

**Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)**

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F06h	0's	Stream & Channel [7:0]

Codec Response for NID=02h~06h, 25h (Output Converters: Front, Surr, Cen/LFE, Side-Surr, Fout DAC, S/PDIF-OUT)

Codec Response for NID=07h~0Ah (Input Converters: LINE ADC, MIX DAC, and S/PDIF-IN)

Bit	Description
31:8	Reserved. Read as 0's
7:4	Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

**Table 60. Verb – Set Converter Stream, Channel (Verb ID=706h)**

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]	0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's
7:4	Set Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel

*Note: This verb assigns stream and channel for output converters (NID=02h~06h, 25h) and input converters (NID=07h~0Ah). Other widgets will ignore this verb.*

## 8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

**Table 61. Verb – Get Pin Widget Control (Verb ID=F07h)**

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 1Fh

(Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, S/PDIF-OUT and S/PDIF-IN)

Bit	Description
31:1	Reserved. Read as 0's
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for a I/O unit) 0: Disabled 1: Enabled
6	Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled
4:3	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.20. Verb – Set Pin Widget Control (Verb ID=707h)

**Table 62. Verb – Set Pin Widget Control (Verb ID=707h)**

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0] for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 1Fh: (Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, S/PDIF-OUT and S/PDIF-IN)

Bit	Description
31:1	Reserved. Read as 0's
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for a I/O unit) 0: Disabled 1: Enabled
6	Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled
4:3	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

## 8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

**Table 63. Verb – Get Unsolicited Response Control (Verb ID=F08h)**

Get Command Format				Codec Response Format	
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>	
CAd=X	Node ID=Xh	Verb ID= F08h	0's	32-bit Response	

Codec Response for NID=01h (GPIO in Audio Function Group), 14h~1Bh (Port A to H)

Bit	Description
31:8	Reserved. Read as 0's
7	Unsolicited Response is Enabled 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's
3:0	Assigned Tag for Unsolicited Response The tag[3:0] is assigned by software to determine which widget generates unsolicited responses

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

## 8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enables a widget to generate an unsolicited response.

**Table 64. Verb – Set Unsolicited Response Control (Verb ID=708h)**

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]	0's for all nodes

'EnableUnsol' in Command Bit[7:0] for NID=01h (GPIO in Audio Function Group), 14h~1Bh (Port A to H)

Bit	Description
31:8	Reserved. Read as 0's
7	Enable Unsolicited Response 0: Disable 1: Enable
6:4	Reserved. Read as 0's
3:0	Tag for Unsolicited Response Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses

## 8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

**Table 65. Verb – Get Pin Sense (Verb ID=F09h)**

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID= F09h	0's	32-bit Response

Codec Response for NID = 14h~1Bh, 1Eh, 1Fh

Bit	Description
31	Presence Detect Status 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance The ALC885 does not support hardware impedance detection. This field is read as 0s.

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)



## 8.24. Verb – Execute Pin Sense (Verb ID=709h)

**Table 66. Verb – Execute Pin Sense (Verb ID=709h)**

Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID= 709h	Right Channel[0]	0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's
0	Right (Ring) Channel Select 0: Sense Left channel (Tip) 1: Sense Right channel (Ring) The ALC885 does not support hardware impedance sensing and will ignore this control.

## 8.25. Verb – Get Volume Knob Widget (Verb ID=F0Fh)

**Table 67. Verb – Get Volume Knob (Verb ID=F0Fh)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=21h	Verb ID= F0Fh	0's	Bit[31:8]=0s, Bit[7:0] is volume

Codec Response for NID = 21h (Volume Knob Widget)

Bit	Description
31:8	Reserved
7	Direct 0: The volume generated by external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately. 1: The volume generated by external HW volume control will directly affect the volume of the amplifier. The ALC885 does not support 'Direct' mode and will respond with 0s for this bit.
6:0	Volume in steps

## 8.26. Verb – Set Volume Knob Widget (Verb ID=70Fh)

**Table 68. Verb – Set Volume Knob (Verb ID=70Fh)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=21h	Verb ID= 70Fh	Bit[7] is 'Direct' control	0's

'Payload' in Command Bit[7:0]

Bit	Description
31:8	Reserved
7	Direct 0: The volume generated by external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately. 1: The volume generated by external HW volume control will directly affect the volume of the amplifier. The ALC885 does not support 'Direct' mode and will respond with 0s for this bit.
6:0	Reserved

## 8.27. Verb – Get Configuration Default (Verb ID=F1Ch)

Reads the 32-bit sticky register for each Pin Widget configured by software.

**Table 69. Verb – Get Configuration Default (Verb ID=F1Ch)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=Xh	Verb ID= F1Ch	0's	32-bit Response

Codec Response for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, and 1Fh

Bit	Description
31:0	32-bit configuration information for each pin widget

*Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).*

## 8.28. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh, e.g., placement and expected default device.

**Table 70. Verb – Set Configuration Default Bytes 0, 1, 2, 3**

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]	0's for all nodes

Note: Supported by Pin Widget NID=14h~1Bh, 1Ch, 1Dh, 1Eh and 1Fh. Other widgets will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

## 8.29. Verb – Get BEEP Generator (Verb ID=F0Ah)

**Table 71. Verb – Get BEEP Generator (Verb ID= F0Ah)**

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID= F1Bh	0's	Divider [7:0]

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is 48kHz/(255*4)=47Hz The highest tone is 48kHz/(1*4)=12kHz A value of 00h in F[7:0] disables internal BEEP generator and allows external PCBEEP input

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.30. Verb – Set BEEP Generator (Verb ID=70Ah)

**Table 72. Verb – Set BEEP Generator (Verb ID= 70Ah)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=71Bh	Divider [7:0]	0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$ The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$ A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

### 8.31. Verb – Get GPIO Data (Verb ID=F15h)

**Table 73. Verb – Get GPIO Data (Verb ID= F15h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=F15h	0's	32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Data. Not supported in the ALC885
1:0	GPIO[1:0] Data The value written (output) or sensed (input) on the corresponding pin if it is enabled

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.32. Verb – Set GPIO Data (Verb ID=715h)

**Table 74. Verb – Set GPIO Data (Verb ID= 715h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=715h	Data [7:0]	0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] output Data. Not supported in the ALC885
1:0	GPIO[1:0] Output Data The value written determines the value driven on a pin that is configured as an output pin

Codec Response for All NID

Bit	Description
31:0	0's

### 8.33. Verb – Get GPIO Enable Mask (Verb ID=F16h)

**Table 75. Verb – Get GPIO Enable Mask (Verb ID= F16h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=F16h	0's	EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Enable mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.34. Verb – Set GPIO Enable Mask (Verb ID=716h)

**Table 76. Verb – Set GPIO Enable Mask (Verb ID=716h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=716h	Enable Mask [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Enable Mask. Not supported in the ALC885
1:0	GPIO[1:0] Enable Mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for All NID

Bit	Description
31:0	0's

### 8.35. Verb – Get GPIO Direction (Verb ID=F17h)

**Table 77. Verb – Get GPIO Direction (Verb ID=F17h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=F17h	0's	Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Direction Control. Not supported in the ALC885
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.36. Verb – Set GPIO Direction (Verb ID=717h)

**Table 78. Verb – Set GPIO Direction (Verb ID=717h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=717h	Direction [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Direction Control. Not supported in the ALC885
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.37. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

**Table 79. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=F19h	0's	UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC885
1:0	GPIO[1:0] Unsolicited Enable mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.38. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

**Table 80. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=719h	UnsolEnable [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC885
1:0	GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's

### 8.39. Verb – Function Reset (Verb ID=7FFh)

**Table 81. Verb – Function Reset (Verb ID=7FFh)**

Command Format (NID=01h)				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd=X	Node ID=01h	Verb ID=7FFh	0's	0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's

Note: The Function Reset command causes all widgets in the ALC885 to return to their power on default state.



## 8.40. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

**Table 82. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)**

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F0Dh/ F0Eh	0's	Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0])

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's
15	Reserved. Read as 0's
14:8	CC[6:0] (Category Code)
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

NID=0Ah (S/PDIF-IN) Response to Get verb (F0Dh)

NID=0Ah (S/PDIF-IN) Response to Get verb (F0Eh)

Bit	Description (part of S/PDIF-IN Channel Status)
31:16	Reserved. Read as 0's
15	Reserved. Read as 0's
14:8	CC[6:0] (Category Code)
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	Reserved
1	In'V'alid. V bit in sub-frame of S/PDIF-IN 0: Data X and Y are valid, or S/PDIF-IN is not locked 1: At least one of data X and Y is invalid
0	Digital Enable. DigEn 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's

## 8.41. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

**Table 83. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)**

Set Command Format (Verb ID=70Xh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Yh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

‘Payload’ in Set Control 1 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

‘Payload’ in Set Control 2 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0’s
6:0	CC[6:0] (Category Code)

‘Payload’ in Set Control 1 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:1	Reserved
0	Digital Enable. DigEn 0: OFF 1: ON

‘Payload’ in Set Control 2 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:0	Reserved. Read as 0’s

*Note: Other widgets will ignore this verb.*

### 8.42. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

32-bit Read/Write register for Audio Function Group (NID=01h)

**Table 84. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)**

Get Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd = X	Node ID=01h	Verb ID=F20h	0s	32-bit Response

Codec Response for NID=01h

Bit	Description
31:16	Subsystem ID[23:8]. (Default=10ECh)
15:8	Subsystem ID[7:0]. (Default=08h).
7:0	Assembly ID[7:0]. (Default=85h).

### 8.43. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

**Table 85. Verb – Set Subsystem ID [31:0] (Verb ID=723h, 722h, 721h, 720h)**

Set Command Format				Codec Response Format
<b>Bit [31:28]</b>	<b>Bit [27:20]</b>	<b>Bit [19:8]</b>	<b>Payload Bit [7:0]</b>	<b>Response [31:0]</b>
CAd = X	Node ID=01h	Verb ID=723h, 722h, 721h, 720h	Label [7:0]	0s for all nodes

Codec Response for all NID

Bit	Description
31:0	0s

## 9. Electrical Characteristics

### 9.1. DC Characteristics

#### 9.1.1. Absolute Maximum Ratings

**Table 86. Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply:					
Digital power for core	DVDD	3.0	3.3	3.6	V
Digital power for HDA link	DVDD-IO*	1.5	3.3	3.6	V
Analog	AVDD**	3.3	5.0	5.25	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts			+125	°C
<b>ESD (Electrostatic Discharge)</b>					
Susceptibility Voltage					
All Pins				3500V	

Note\*: The digital link power DVDD-IO must be lower than the digital core power DVDD.

Note\*\*: The standard testing condition before shipping is AVDD = 5.0V unless specified. Customer designing with a different AVDD should contact Realtek technical support representatives for special testing support.

#### 9.1.2. Threshold Voltage

DVDD= 3.3V±5%, T<sub>ambient</sub>=25°C, with 50pF external load.

**Table 87. Threshold Voltage**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V <sub>in</sub>	-0.30	-	DVDD +0.30	V
Low Level Input Voltage (HDA link)	V <sub>IL</sub>	-	-	0.30* DVDDIO	V
High Level Input Voltage (HDA link)	V <sub>IH</sub>	0.65* DVDDIO	-	-	V
Low Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V <sub>IL</sub>	-	-	0.44*DVDD (1.45)	V
High Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V <sub>IH</sub>	0.56* DVDD (1.85)	-	-	V
High Level Output Voltage	V <sub>OH</sub>	0.9*DVDD		-	V
Low Level Output Voltage	V <sub>OL</sub>	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	μA
Output Leakage Current (Hi-Z)	-	-10	-	10	μA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

### 9.1.3. Digital Filter Characteristics

**Table 88. Digital Filter Characteristics**

Filter	Description	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	0.45*Fs	kHz
	Stopband	0.60*Fs			kHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		±0.02		dB
DAC Lowpass Filter	Passband	0	-	0.45*Fs	kHz
	Stopband	0.60*Fs			kHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		±0.02		dB

Note: Fs=Sample rate

### 9.1.4. S/PDIF Input/Output Characteristics

DVDD= 3.3V, T<sub>ambient</sub>=25°C, with 75Ω external load.

**Table 89. S/PDIF Input/Output Characteristics**

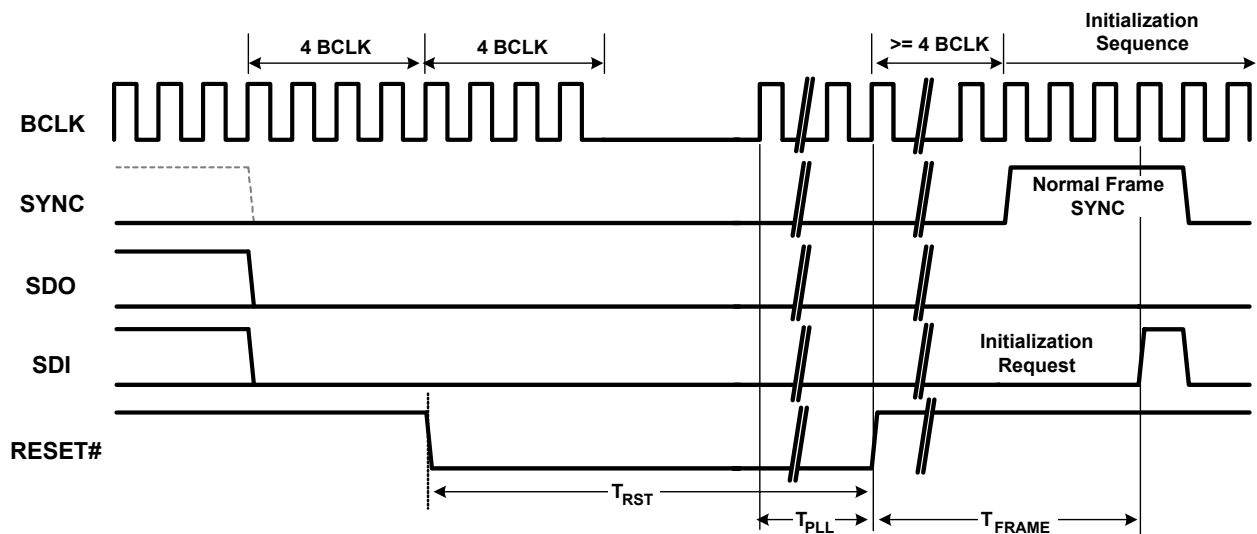
Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V <sub>OH</sub>	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V <sub>OL</sub>	-	0	0.3	V
S/PDIF-IN High Level Input	V <sub>IH</sub>	1.85	-	-	V
S/PDIF-IN Low Level Input	V <sub>IL</sub>	-	-	1.45	V
S/PDIF-IN Bias Level	V <sub>t</sub>	-	1.65	-	V

## 9.2. AC Characteristic

### 9.2.1. Link Reset and Initialization Timing

**Table 90. Link Reset and Initialization Timing**

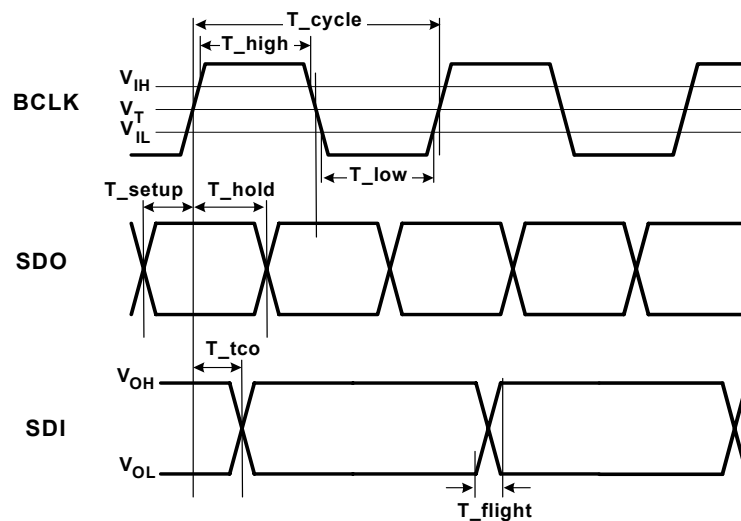
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	$T_{RST}$	1.0	-	-	$\mu\text{s}$
RESET# Inactive to BCLK Startup delay for PLL ready time	$T_{PLL}$	20	-	-	$\mu\text{s}$
SDI Initialization Request	$T_{FRAME}$	-	-	1	Frame Time


**Figure 15. Link Reset and Initialization Timing**

## 9.2.2. Link Timing Parameters at the Codec

**Table 91. Link Timing Parameters at the Codec**

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency		-	24.0	-	MHz
BCLK Period	$T_{\text{cycle}}$	-	41.67	-	ns
BCLK Jitter	$T_{\text{jitter}}$	-	-	2.0	ns
BCLK High Pulse Width	$T_{\text{high}}$	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	$T_{\text{low}}$	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	$T_{\text{setup}}$	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	$T_{\text{hold}}$	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1: 50pF external load)	$T_{\text{tco}}$	-	7.5	8.0	ns
SDI Flight Time	$T_{\text{flight}}$	-	2.0	-	ns


**Figure 16. Link Signals Timing**



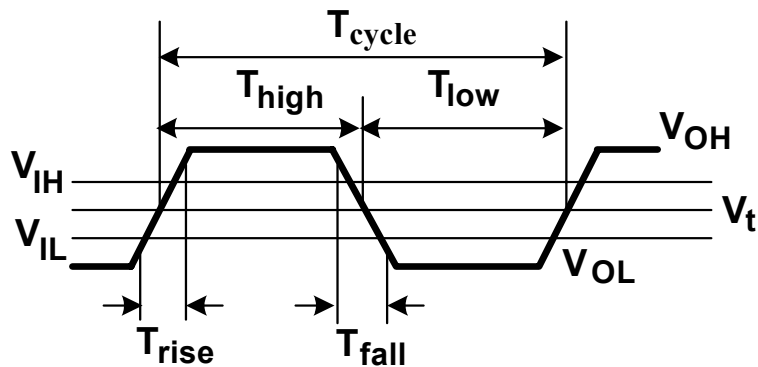
### 9.2.3. S/PDIF Output and Input Timing

**Table 92. S/PDIF Output and Input Timing**

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency	-	-	3.072	-	MHz
S/PDIF-OUT Period <sup>*1</sup>	$T_{cycle}$	-	325.6	-	ns
S/PDIF-OUT Jitter	$T_{jitter}$	-	-	4	ns
S/PDIF-OUT High Level Width	$T_{High}$	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width	$T_{Low}$	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	$T_{rise}$	-	2.0	-	ns
S/PDIF-OUT Falling Time	$T_{fall}$	-	2.0	-	ns
S/PDIF-IN Period <sup>*2</sup>	$T_{cycle}$	-	325.6	-	ns
S/PDIF-IN Jitter	$T_{jitter}$	-	-	10	ns
S/PDIF-IN High Level Width	$T_{High}$	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)
S/PDIF-IN Low Level Width	$T_{Low}$	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)

<sup>\*1</sup>: Bit parameters for 48kHz sample rate of S/PDIF-OUT

<sup>\*2</sup>: Bit parameters for 48kHz sample rate of S/PDIF-IN


**Figure 17. Output and Input Timing**

### 9.2.4. Test Mode

The ALC885 does not support codec test mode or Automatic Test Equipment (ATE) mode.

### 9.3. Analog Performance

- Standard Test Conditions
- $T_{\text{ambient}}=25\text{ }^{\circ}\text{C}$ , DVDD=3.3V  $\pm$ 5%, AVDD=5.0V $\pm$ 5%
  - 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
  - 10K $\Omega$ /50pF load; Test bench Characterization BW:10Hz~22kHz

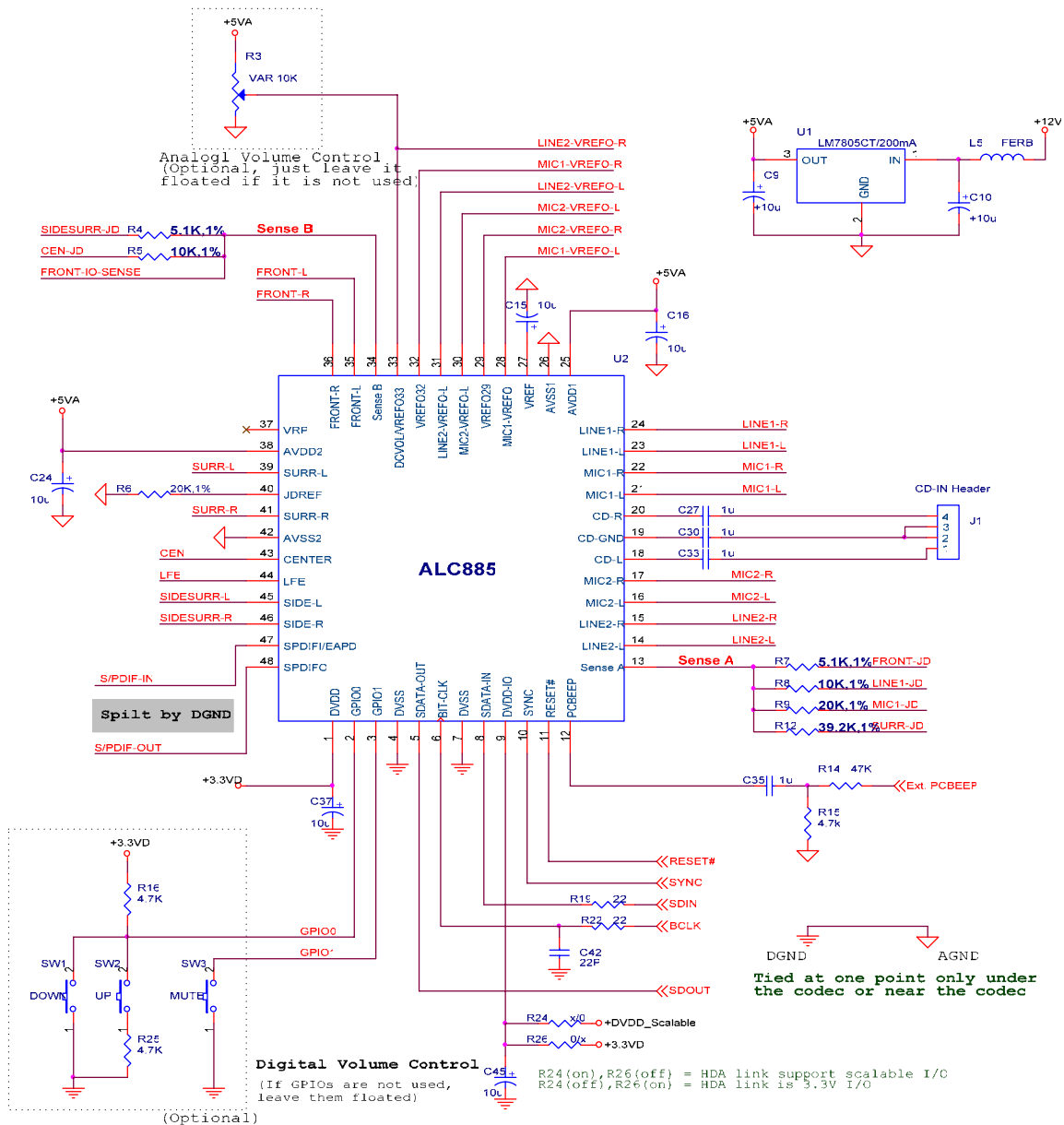
**Table 93. Analog Performance**

Parameter	Min	Typical	Max	Units
Full Scale Input Voltage				
All Inputs (gain=0dB)	-	1.4	-	Vrms
ADC	-	1.4	-	Vrms
Full Scale Output Voltage				
DAC	-	1.4	-	Vrms
Headphone Amplifier Output@32 $\Omega$ Load	-	1.0	-	Vrms
Dynamic Range with -60dB signal (A-Weight)				
ADC	-	101	-	dB FSA
DAC	-	106	-	dB FSA
Headphone Amplifier Output@32 $\Omega$ Load	-	106	-	dB FSA
THD+N with -3dB signal (No A-Weight)				
ADC	-	-90	-	dB FS
DAC	-	-95	-	dB FS
Headphone Amplifier Output@32 $\Omega$ Load	-	-75	-	dB FS
Magnitude Response (10K $\Omega$ load)				
All DAC @Fs=48KHz (FR= $\pm$ 0.05dB)	10	-	21,792	Hz
All DAC @Fs=96KHz (FR= $\pm$ 0.05dB)	10	-	43,584	Hz
All DAC @Fs=192KHz (FR= $\pm$ 0.05dB)	10	-	87,168	Hz
All ADC @Fs=48KHz (FR= $\pm$ 0.05dB)	10	-	19,200	Hz
All ADC @Fs=96KHz (FR= $\pm$ 0.05dB)	10	-	38,400	Hz
All ADC @Fs=192KHz (FR= $\pm$ 0.05dB)	10	-	76,800	Hz
Power Supply Rejection	-	-60	-	dB
Amplifier Gain Step	-	1.0	-	dB
Channel Separation (Crosstalk)	-	-100	-	dB
Input Impedance (gain=0dB)	-	47	-	K $\Omega$
Output Impedance				
Amplified Output	-	1	-	$\Omega$
Non-amplified Output	-	100	-	$\Omega$
Digital Power Supply Current (normal/DVD-Audio)				
DVDD=3.3V	-	40/70	-	mA
Digital Power Supply Current (power down mode)				
DVDD=3.3V	-	-	1000	$\mu$ A
Analog Power Supply Current (normal operation)				
AVDD=5.0V/3.3V	-	70/46	-	mA
Analog Power Supply Current (power down mode)				
AVDD=5.0V/3.3V	-	-	900/500	$\mu$ A
VREFOUTx Output Voltage	2.25	2.50	3.75	V
VREFOUTx Output Current	-	5	-	mA

# 10. Application Circuits

The ALC885 is in a 48-pin LQFP package and is pin-to-pin compatible with the ALC882, ALC883, and ALC888. A board designed for those Codex can use the ALC885 directly.

To get the best compatibility in hardware design and software driver, any modification should be confirmed by Realtek. Realtek may update the latest application circuits onto our web site ([www.realtek.com.tw](http://www.realtek.com.tw)) without modifying this datasheet.

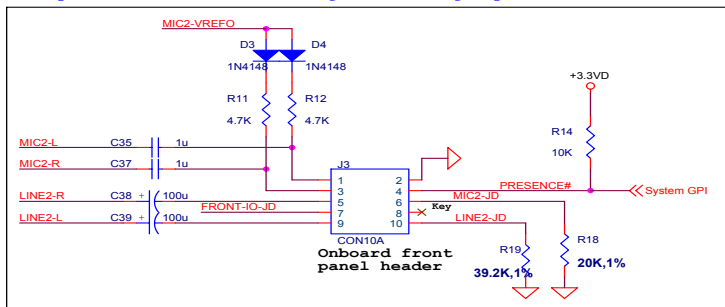


**Figure 18. Filter Connection**

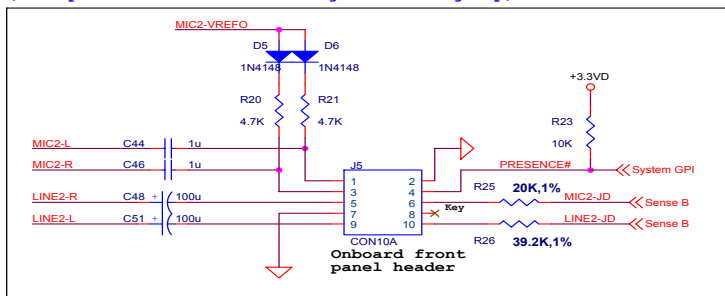
Option 1 in Figure 19 comes from by Intel’s front panel IO connectivity design guide. A drawback of this option is that the ports connected to the front panel must use the same jack detection pin. According to the HD Audio standard specification, ports A/B/C/D use ‘Sense A’ as the jack detect pin; ports E/F/G/H use ‘Sense B’ as the jack detect pin. This is not a good option when the system integrators want to use port-A (pin 39/41) and port-F (pin 16/17) to be the front panel ports, as ‘Sense A’ and ‘Sense B’ cannot be tied together.

Option 2 in Figure 19 shows an alternative front panel header design that is also compatible with standard front panel I/O cable. The option 2 header design lets the two ports use an individual sense pin, and is compatible with current HD Audio front panel cable.

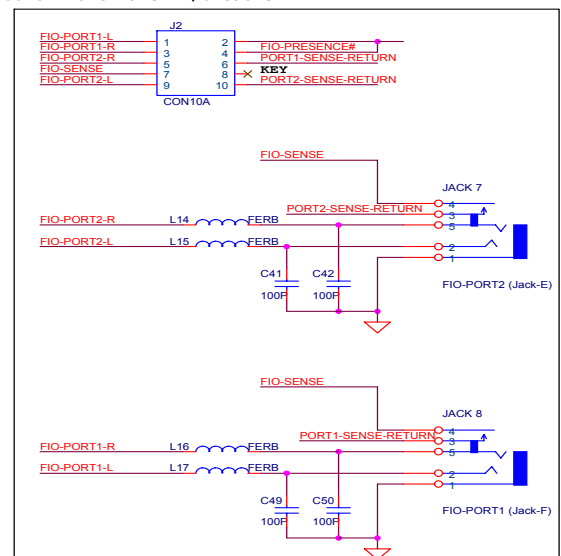
**Option 1: Follow Intel's HD Audio front panel header design**  
(Two ports must be in the same jack detect group)



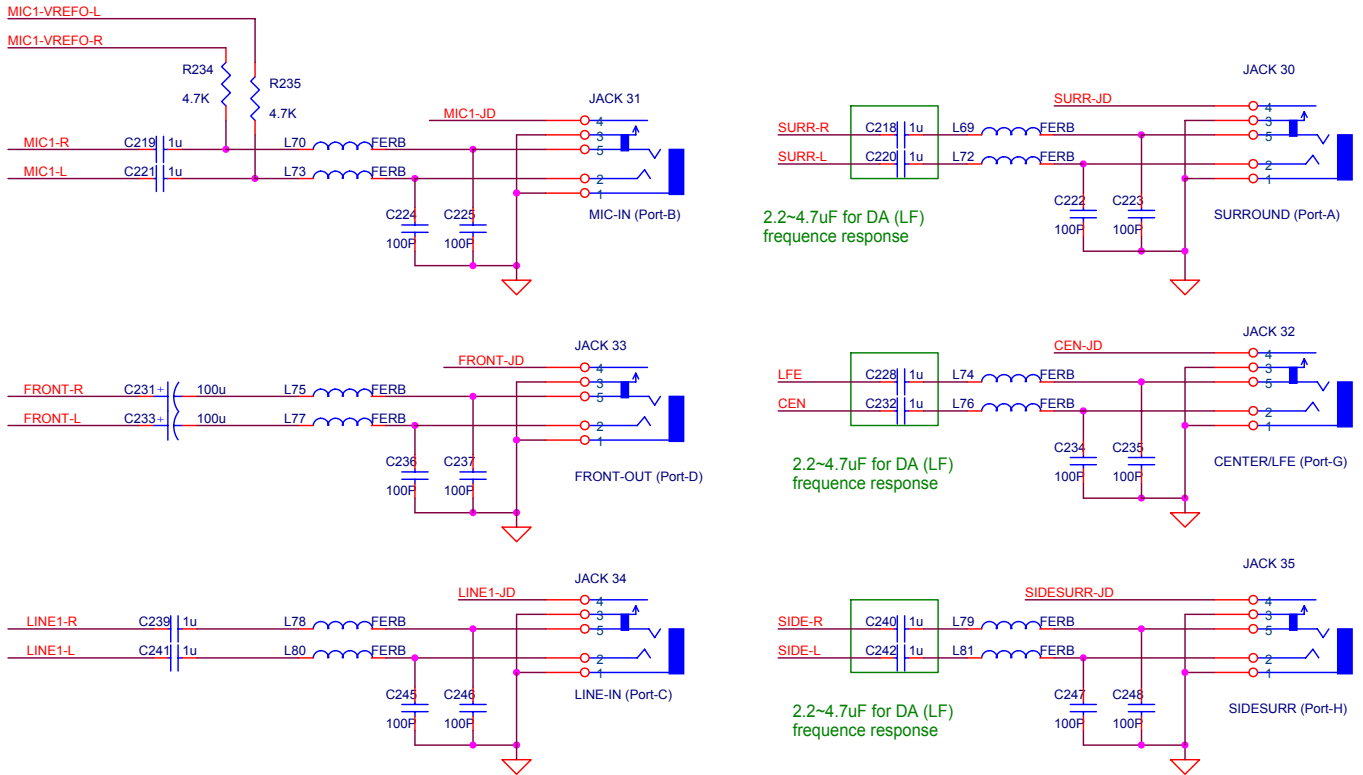
**Option 2: A more flexible front panel header**  
(Each port can be in different jack detect group)



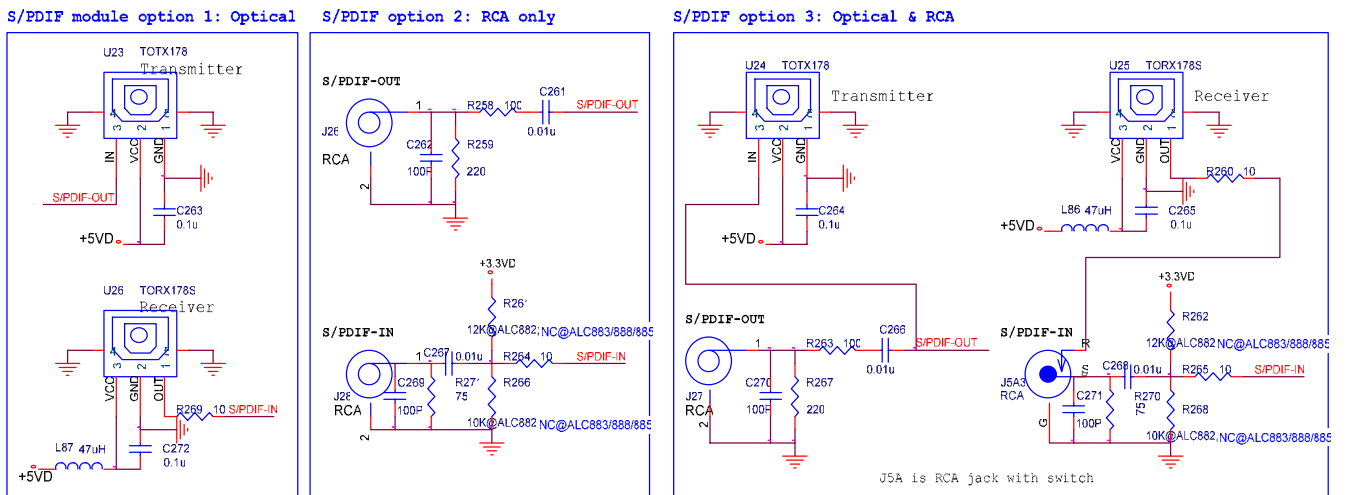
**HD Audio Front Panel I/O Cable**



**Figure 19. Front Panel Header Connection**



**Figure 20. Jack Connection on Rear Panel**



**Figure 21. S/PDIF Input/Output Connection**

## 11. Application Supplements

### 11.1. Standby Mode

In standby mode the ALC885 turns on all DC bias on all input and output ports (NID=14h~1Bh). This is a special application to avoid ‘PoP’ noise while in power on and power off periods. Table 94 shows the DC bias state when Standby mode is enabled.

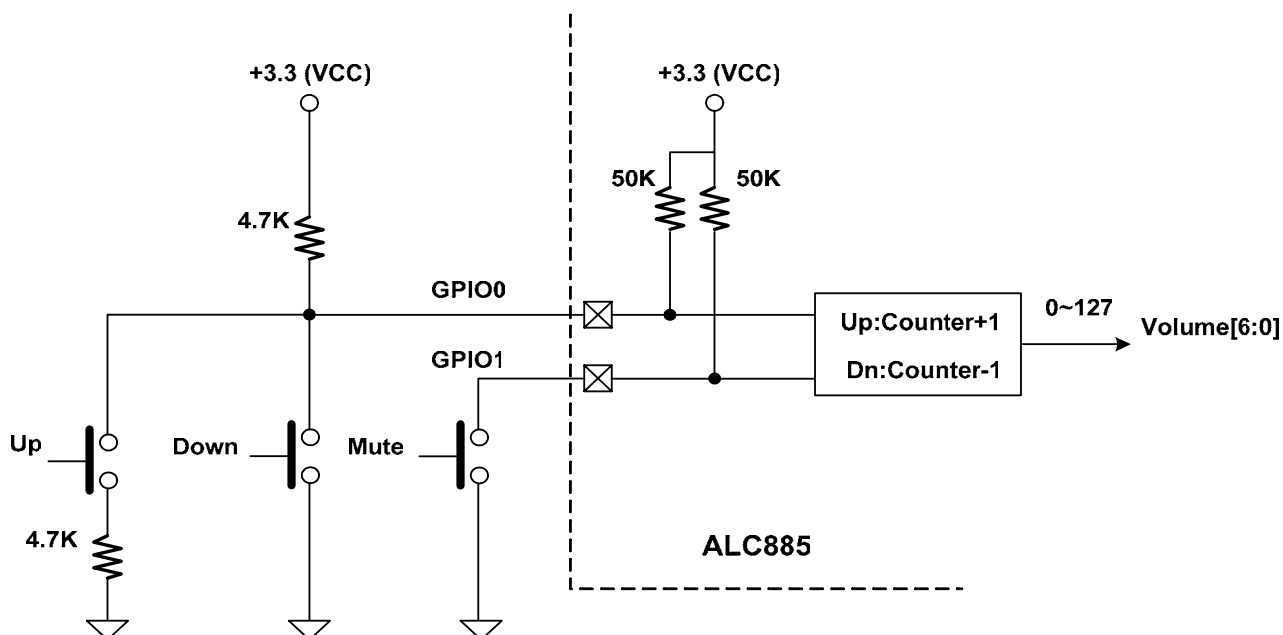
**Table 94. Standby Mode**

+3.3V on DVDD (Pin-1)	+5VA on AVDD	Operation Mode
No (<2.0V)	No	Shut Down
No (<2.0V)	Yes	Standby Mode
Yes (>2.0V)	No	Normal
Yes (>2.0V)	Yes	Normal

### 11.2. Volume Knob Control

#### 11.2.1. GPI Volume Control via GPIO0 (Up/Down), GPIO1 (Mute)

Low pulses, generated at GPIO0 and GPIO1, are used to calculate the Up and Down count into 7 bits of volume step. ‘Mute’ is also sampled by 512\*SYNC to toggle the mute status. Hardware will not adjust volume; the count value will be reported by unsolicited response to software.



**Figure 22. GPI Volume Control Implementation**

### 11.2.2. Volume Control by External Variable Resistor

A 5-bit resolution ADC operating at  $64 \times \text{SYNC}$  clock rate is used to convert the DC level on VAR into 32 steps for the Volume knob. Hardware will not directly change the volume, the DC level change will be reflected to software by unsolicited response in every  $64 \text{ SYNC} (=64 \times 20.84 \mu\text{sec})$

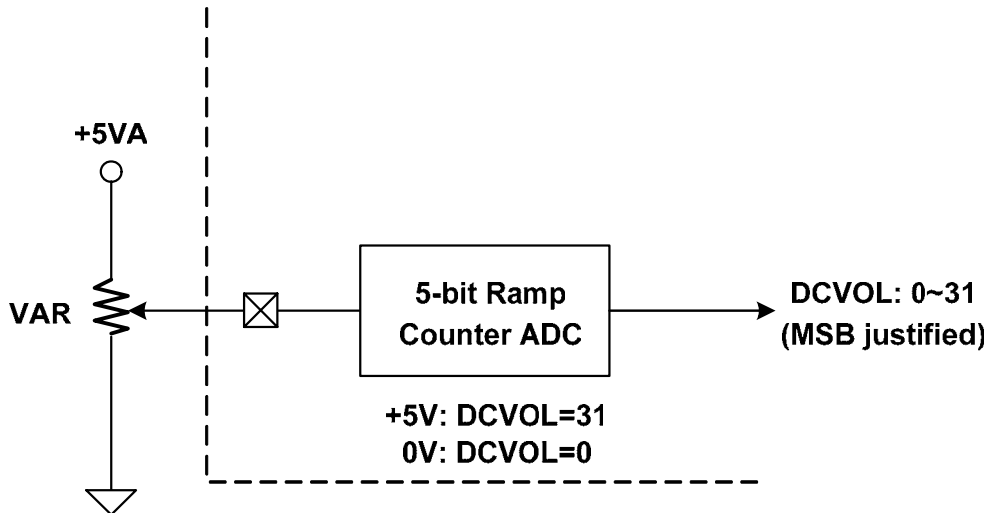


Figure 23. Volume Control by External Variable Resistor

Table 95. Volume Code Corresponding to DC Level at Pin 33

Input DC Voltage	Volume Code	Input DC Voltage	Volume Code	Input DC Voltage	Volume Code	Input DC Voltage	Volume Code
$95.0\% < DC$	1F	$71.0\% < DC \leq 74.0\%$	17	$47.0\% < DC \leq 50.0\%$	0F	$23.0\% < DC \leq 26.0\%$	07
$92.0\% < DC \leq 95.0\%$	1E	$68.0\% < DC \leq 71.0\%$	16	$44.0\% < DC \leq 47.0\%$	0E	$20.0\% < DC \leq 23.0\%$	06
$89.0\% < DC \leq 92.0\%$	1D	$65.0\% < DC \leq 68.0\%$	15	$41.0\% < DC \leq 44.0\%$	0D	$17.0\% < DC \leq 20.0\%$	05
$86.0\% < DC \leq 89.0\%$	1C	$62.0\% < DC \leq 65.0\%$	14	$38.0\% < DC \leq 41.0\%$	0C	$14.0\% < DC \leq 17.0\%$	04
$83.0\% < DC \leq 86.0\%$	1B	$59.0\% < DC \leq 62.0\%$	13	$35.0\% < DC \leq 38.0\%$	0B	$11.0\% < DC \leq 14.0\%$	03
$80.0\% < DC \leq 83.0\%$	1A	$56.0\% < DC \leq 59.0\%$	12	$32.0\% < DC \leq 35.0\%$	0A	$8.0\% < DC \leq 11.0\%$	02
$77.0\% < DC \leq 80.0\%$	19	$53.0\% < DC \leq 56.0\%$	11	$29.0\% < DC \leq 32.0\%$	09	$5.0\% < DC \leq 8.0\%$	01
$74.0\% < DC \leq 77.0\%$	18	$50.0\% < DC \leq 53.0\%$	10	$26.0\% < DC \leq 29.0\%$	08	$DC \leq 5.0\%$	00

### 11.3. Digital Microphone Implementation

This section describes the ALC885 digital microphone implementation. There is one Clock output pin and 1 Data input pin in the ALC885. The ALC885 provides the clock signal to the digital microphone. When the digital microphone receives the external sound input, it converts the analog signals to digital in a 1-bit format. The 1-bit data is delivered to the codec through the data input pin. The Digital Filter in the audio codec converts the 1-bit data stream into Pulse Code Modulation (PCM) data. The PCM data is sent to the HDA controller through the HDA link.

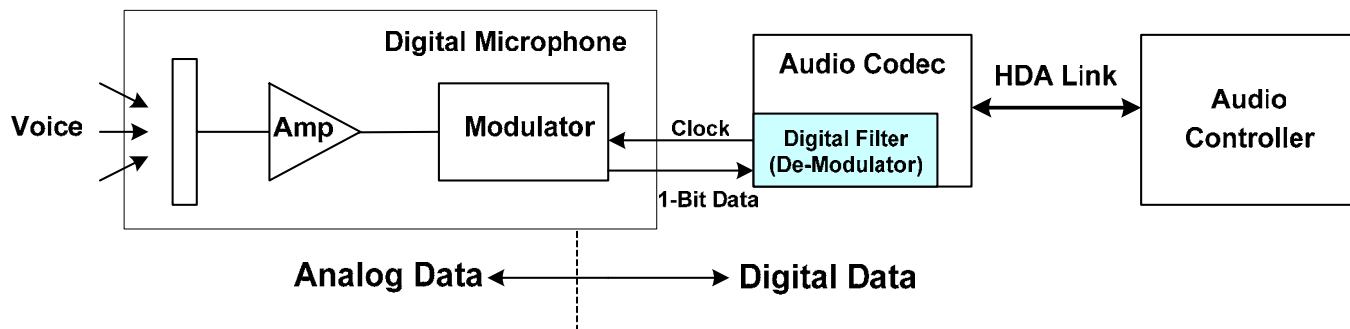


Figure 24. Digital Microphone Implementation-1

The ALC885 supports a two-wire interface for the digital microphone and operates in single channel (mono type) or stereo channels (stereo mode) of digital microphones. One pin is clock output to the digital microphone, and the other is a serial pin. The default clock output is 2.048MHz.

In Type 1 (Figure 25), the ALC885 uses one data pin to support mono input from digital microphones with LMV1024 (L), SPD0205ND (L), or AKU2000 (L).

In Type 2 (Figure 25), the ALC885 uses one data pin to support stereo inputs from digital microphones with LMV1024/1026 (L/R), SPD0205ND (L & R), or AKU2000 (L & R).

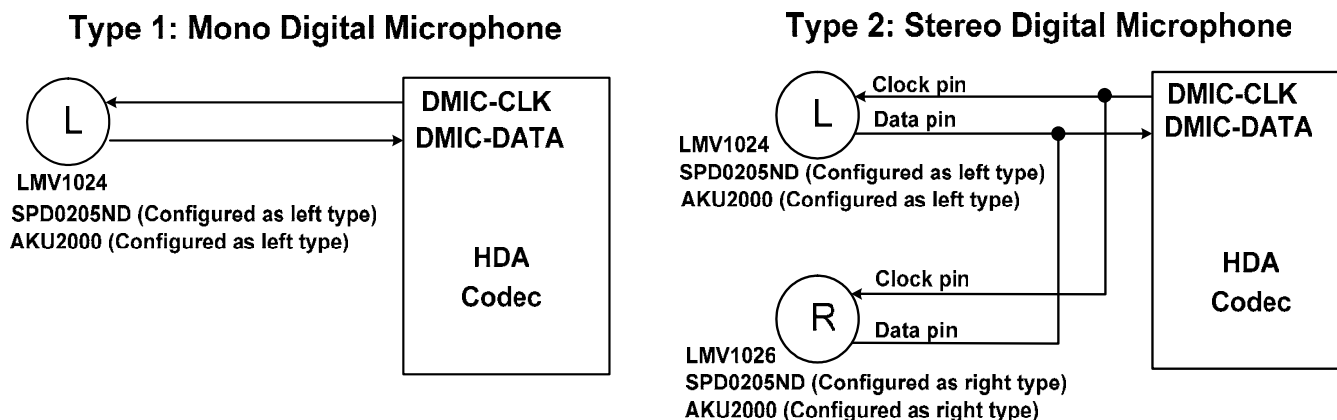
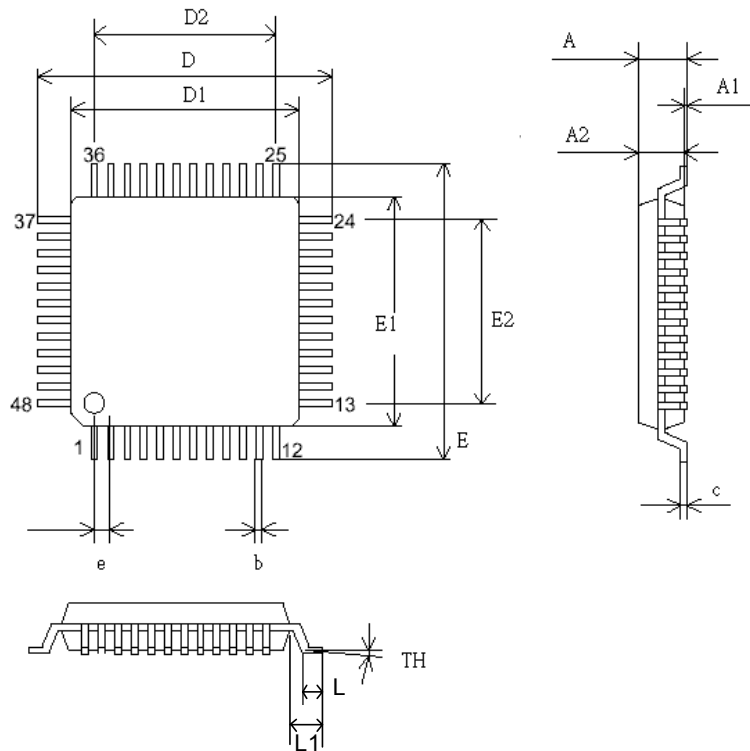


Figure 25. Digital Microphone Implementation-2



## 12. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

## 13. Ordering Information

**Table 96. Ordering Information**

<b>Part Number</b>	<b>Description</b>	<b>Status</b>
ALC885-GR	LQFP-48 with 'Green' package	MP
ALC885M-GR	ALC885-GR + Dolby <sup>®</sup> Master Studio <sup>™</sup> (software feature)	MP

*Note 1: See page 6 for 'Green' package and version identification.*

*Note 2: Above parts are tested under AVDD = 5.0V. Customers requesting lower AVDD support should contact Realtek sales representatives or agents.*

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