8A, 23V Synchronous Step-Down Converter with 3.3V/5V LDO

General Description

The RT6228A/B/C is an advanced constant on-time (ACOT®) mode synchronous buck converter. The main control loop of the RT6228A/B/C using an advanced constant on-time (ACOT®) mode control which provides a very fast transient response. The RT6228A/B operates from 4.5V to 23V input voltage and the RT6228C operates from 5.1V to 23V. For the RT6228A, the output voltage can be programmed between 0.6V to 5.1V.

Ordering Information

RT6228A/B/C □□

- Package Type
  QUF : UQFN-12HL 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage
  A : Adjustable
  B : 3.3V
  C : 5.1V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

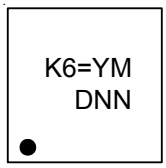
- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Features

- **4.5V to 23V (RT6228A/B) and 5.1V to 23V (RT6228C) Input Voltage Range 8A Output Current**
- **ACOT® Mode Performs Fast Transient Response**
- **ACOT® Architecture to Enable All MLCC Output Capacitor Usage**
- **Fixed 750kHz (RT6228C) and 500kHz (RT6228A/B) Switching Frequency**
- **High Efficient Internal Power MOSFET Switch-20mΩ (High-Side) and 10mΩ (Low-Side)**
- **Adjustable Output Voltage from 0.6V to 5.1V (RT6228A)**
- **Fixed 3.3V (RT6228C) LDO Output Supplies 100mA**
- **Pre-biased Soft-Start**
- **Cycle-by-Cycle Over-Current Protection**
- **Input Under-Voltage Lockout**
- **Thermal Shutdown Protection**
- **Output Over-/Under-Voltage Protection**
- **Ultrasonic Mode (USM)**
- **300kHz CLK for External Charge Bump**

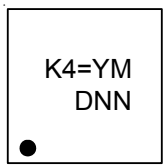
Marking Information

RT6228AGQUF



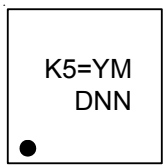
K6= : Product Code
YMDNN : Date Code

RT6228BGQUF



K4= : Product Code
YMDNN : Date Code

RT6228CGQUF



K5= : Product Code
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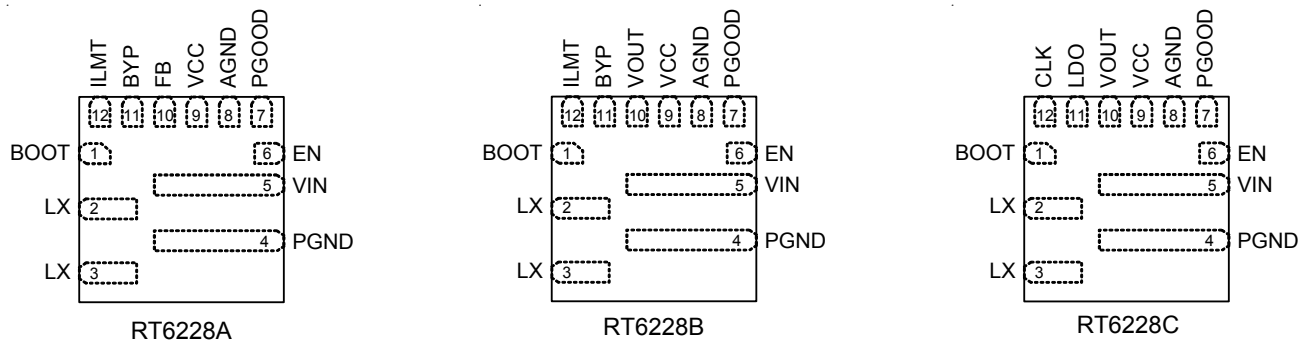
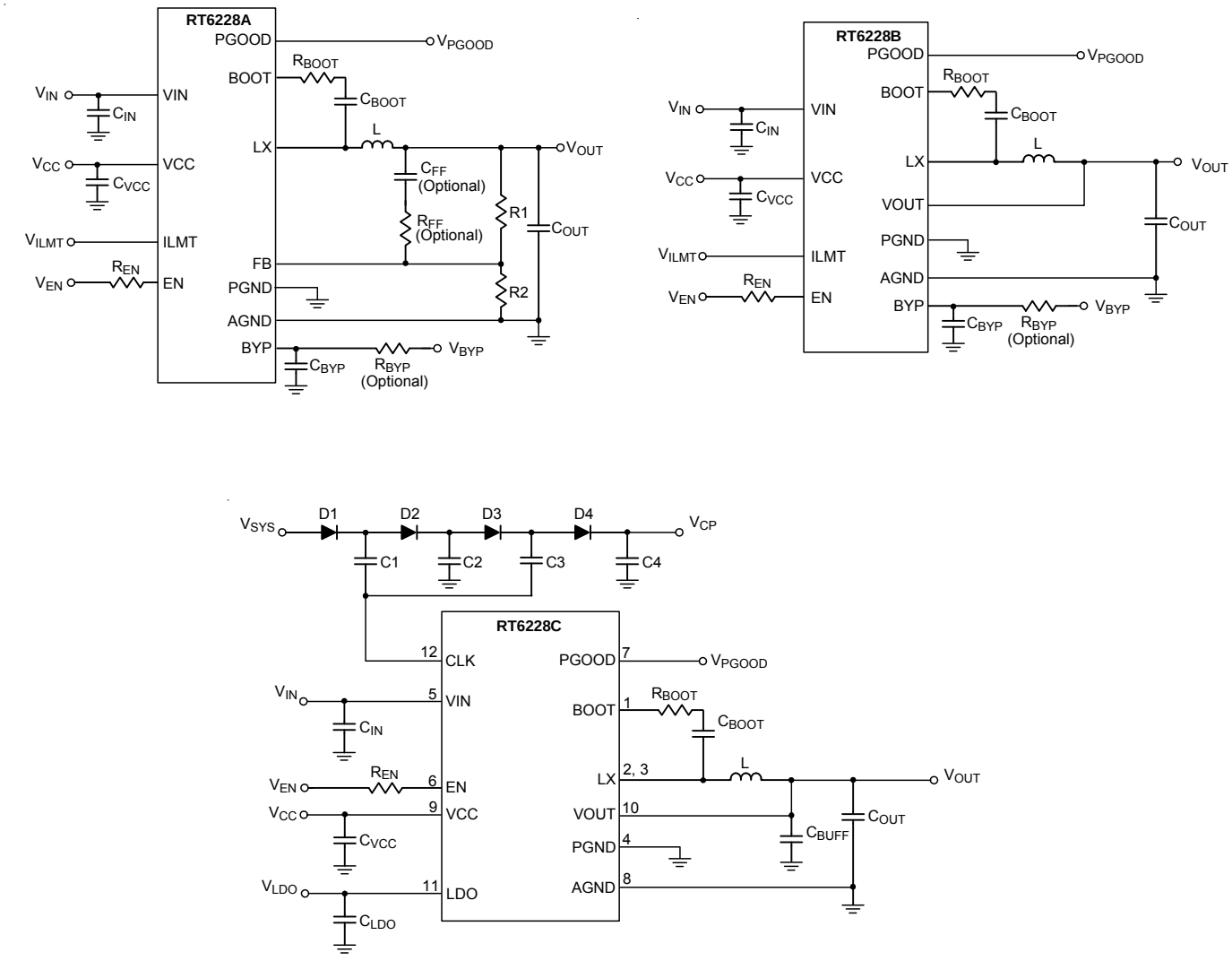
Pin Configuration

(TOP VIEW)



Simplified Application Circuit

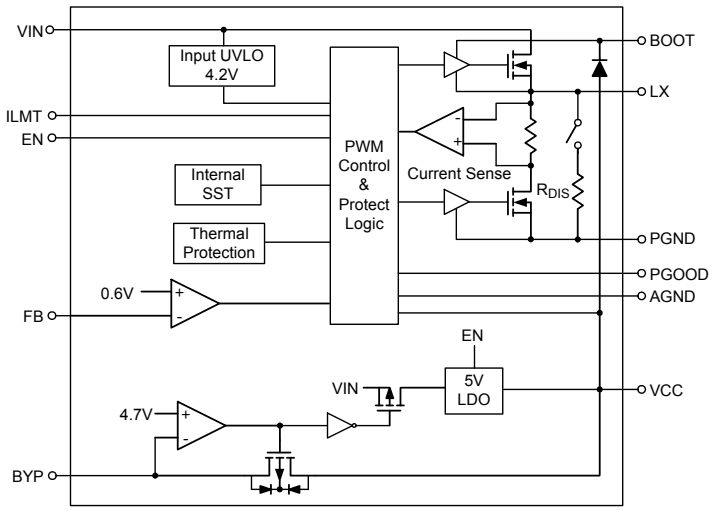


Functional Pin Description

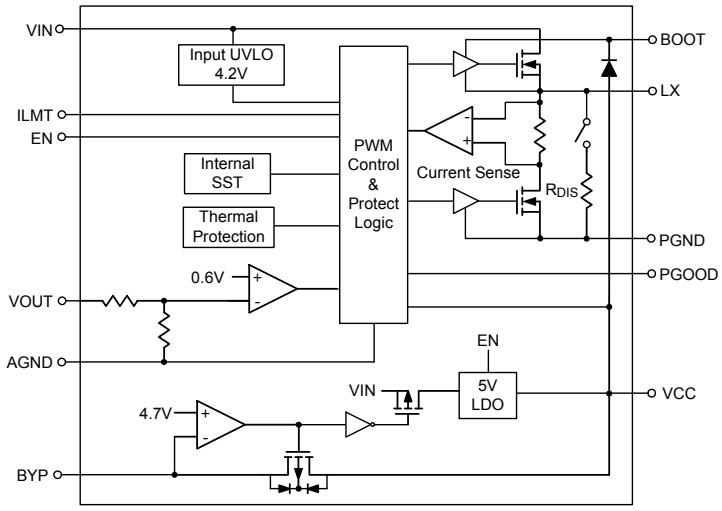
Pin No.	Pin Name	Pin Function
1	BOOT	Boot-strap pin. Supply high-side gate driver. A 0.1μF ceramic capacitor and at least 10Ω R_{BOOT} are connected between this pin and LX pin.
2,3	LX	Inductor pin. Connect this pin to the switching node of inductor.
4	PGND	Power ground.
5	VIN	Input pin. Decouple this pin to GND pin with at least 10μF ceramic cap.
6	EN (RT6228A)	Enable control. Pull this pin high to turn on the Buck. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 2.3V and 23V, it will enter USM mode, if EN pin voltage is between 0.8V and 1.7V, then it is normal mode.
	EN (RT6228B)	Enable control. Pull this pin high to turn on the Buck. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 2.3V and 23V, it will enter USM mode, if EN pin voltage is between 0.8V and 1.7V, then it is normal mode.
	EN (RT6228C)	Enable control. Pull this pin high to turn on the Buck and CLK. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 2.3V and 23V, it will enter USM mode, if EN pin voltage is between 0.8V and 1.7V, then it is normal mode.
7	PGOOD	Power good Indicator. Open drain output when the output voltage is higher than 90% of regulation point.
8	AGND	Analog ground.
9	VCC	5V linear regulator output for internal control circuit. A capacitor (typical 1μF) should be connected to AGND. Don't connect to external Load.
10	FB (RT6228A)	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
	VOUT (RT6228B)	Output pin. Connect to the output of DC-DC regulator.
	VOUT (RT6228C)	Output pin. Connect to the output of DC-DC regulator. The pin also provide the bypass input for 3.3V LDO.
11	BYP (RT6228A)	Bypass input for the internal LDO. BYP is externally connected to the output of switching regulator. When the BYP voltage rises above the bypass switch turn-on threshold, the LDO regulator shuts down and the VCC pin is connected to the BYP pin through an internal switch.
	BYP (RT6228B)	Bypass input for the internal LDO. BYP is externally connected to the output of switching regulator. When the BYP voltage rises above the bypass switch turn-on threshold, the LDO regulator shuts down and the VCC pin is connected to the BYP pin through an internal switch.
	LDO (RT6228C)	Internal 3.3V LDO output. Bypass a capacitor to GND. This pin is also capable sourcing 100mA current for external load.
12	ILMT (RT6228A)	Current limit setting pin. The current limit is set to 8A, 10A or 12A when this pin is pull low, floating or pull high respectively.
	ILMT (RT6228B)	Current limit setting pin. The current limit is set to 8A, 10A or 12A when this pin is pull low, floating or pull high respectively.
	CLK (RT6228C)	300kHz CLK output to drive the external charge pump.

Functional Block Diagram

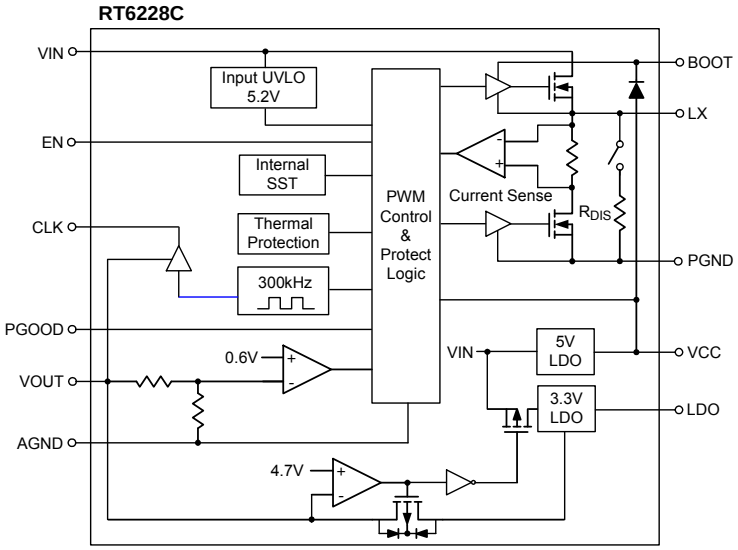
RT6228A



RT6228B



RT6228C



Operation

Overall

The RT6228A/B/C is an advanced constant on-time (ACOT®) mode synchronous buck converter. The main control loop of the RT6228A/B/C using an ACOT® mode control which provides a very fast transient response.

Internal VCC Regulator

The RT6228A/B/C includes a 5V linear regulator (VCC). The VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads.

VCC Bypass Function (RT6228A/B)

When PGOOD is pulled high and BYP pin of RT6228A/B voltage is above 4.7V, an internal 3Ω P-MOSFET switch connects VCC to the BYP pin while the VCC linear regulator is simultaneously turned off.

LDO (RT6228C)

The RT6228C includes a 3.3V 100mA linear regulators (LDO). When VOUT is higher than the switch over threshold 4.7V (RT6228C), an automatic circuit will change the power source of linear regulator from VIN path to VOUT path.

Soft-Start

The RT6228A/B/C provides an internal soft-start function to prevent large inrush current and output voltage overshoot. The typical soft-start duration is around 0.6ms.

Over-Current Limit

The RT6228A/B/C current limit is fixed 9A (RT6228C) or adjustable (8A, 10A, 12A) by ILMT pin (RT6228A/B) and it is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. If output voltage drops below the output under-voltage protection level, the RT6228A/B/C will stop switching to avoid excessive heat.

Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The RT6228A/B/C includes output over-voltage protection (OVP) and output under-voltage protection (UVP). If the output voltage rises above OVP threshold or drops below UVP threshold for longer than 20μs (typical), the OVP or UVP function is triggered.

Power Good

The power good output is an open drain output that requires a pull-up resistor. PGOOD will be pulled high after soft-start is over and the output reaches 90% of its set voltage. There is a 10μs delay built into PGOOD circuitry to prevent false transition.

CLK Generator (RT6228C)

Provide a 300kHz VCLK signal to drive external charge pump circuit.

Absolute Maximum Ratings (Note 1)

- Supply Voltage,VIN ---------- –0.3V to 27V
- Enable Pin Voltage, V_{EN} ---------- –0.3V to 27V
- FB Pin Voltage, V_{FB} (RT6228A) ---------- –0.3V to 4.5V
- VOUT Pin Voltage, V_{OUT} (RT6228B) ---------- –0.3V to 4.5V
- VOUT Pin Voltage, V_{OUT} (RT6228C) ---------- –0.3V to 6V
- Switch Voltage, V_{LX} ---------- –0.3V to (V_{IN} + 0.3V)
  <30ns ---------- –5V to 28V
- Boot Voltage, V_{BS} ---------- (V_{LX} – 0.3V) to (V_{LX} + 6V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-12HL 3x3 (FC) ---------- 2.79W
- Package Thermal Resistance (Note 2)
  UQFN-12HL 3x3 (FC), θ_{JA} ---------- 35.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage VIN (RT6228A/B) ---------- 4.5V to 23V
- Supply Input Voltage VIN (RT6228C) ---------- 5.1V to 23V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	RT6228A/B	4.5	--	23	V
		RT6228/C	5.1	--	23	
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0 (RT6228A/B)	2.5	5	10	μA
		V_{EN} = 0 (RT6228C)	40	50	60	
Supply Current (Quiescent)	I_Q	I_{OUT} = 0, V_{OUT} = V_{SET} x 105%, V_{EN} = 1V	80	100	130	μA
Logic Threshold						
EN Input Low Voltage	V_{ENL}		--	--	0.4	V
EN Input High Voltage	V_{ENH}		0.8	--	--	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Ultra-Sonic Mode	V_{EN}			2.3	--	--	V
Normal Mode	V_{EN}			--	--	1.7	V
Output Voltage							
Output Voltage Setpoint	V_{OUT}	RT6228B		3.267	3.3	3.333	V
		RT6228C		5.049	5.1	5.151	
VCC Regulator Voltage	V_{CC}			--	5	--	V
Feedback Voltage							
Feedback Reference Voltage	V_{REF}	(RT6228A)		0.594	0.6	0.606	V
Feedback Current	I_{FB}	V_{FB} = 4V (RT6228A)		–50	--	50	nA
On Resistance							
High-Side Switch On Resistance	$R_{DS(ON)\_H}$			14	20	26	mΩ
Low-Side Switch On Resistance	$R_{DS(ON)\_L}$			8	10	12	mΩ
Discharge FET Ron	R_{DIS}			40	50	63	Ω
Current Limit							
Top FET Current Limit	I_{LIM_T}			--	15	--	A
Bottom FET Current Limit	I_{LIM_B}	RT6228C		9	10.4	11.8	A
Bottom FET Current Limit	I_{LIM_B}	ILMT = ”0”	RT6228A/B	8	9.6	12	A
		ILMT = Floating		10	12	15	
		ILMT = ”1”		12	14.9	17.8	
ILMT Rising Threshold	V_{ILMTH}			V_{CC} – 0.8	--	V_{CC}	V
ILMT Falling Threshold	V_{ILMTL}			--	--	0.8	V
Oscillator Frequency							
Oscillator Frequency	f_{OSC}	RT6228A/B		0.42	0.5	0.58	MHz
		RT6228C		0.62	0.75	0.9	MHz
On-Time Timer Control							
Minimum On-Time	t_{ON_MIN}	V_{IN} = $V_{IN(MAX)}$		40	50	80	ns
Minimum Off-Time	t_{OFF_MIN}	RT6228A		300	400	600	ns
Minimum Off-Time	t_{OFF_MIN}	RT6228B/C		150	200	300	ns
Ultrasonic Mode							
Operation Period	t_{USM}			20	30	40	μs
Soft-Start							
Soft-Start Time	t_{SS}	From EN high to PGOOD high		1.3	1.65	2	ms
Output Rising Time	t_R	From 10% to 90% VOUT		--	0.6	--	ms
UVLO							
Input UVLO Threshold	V_{UVLO}	Wake up RT6228A/B		--	--	4.5	V
		Wake up RT6228C		--	--	5.4	
UVLO Hysteresis	V_{HYS}			--	0.3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Over-Voltage Protection						
Output Over-Voltage Threshold		V_{OUT} rising	115	120	125	%
Output Over-Voltage Hysteresis			--	3	--	%
Output Over-Voltage Delay Time			--	20	--	μs
Output Under-Voltage Protection						
Output Under-Voltage Threshold		V_{FB} falling	54	60	64	%
Output Under-Voltage Delay Time		FB forced below UV threshold	--	20	--	μs
UV Blank Time		From EN high	--	1.65	--	ms
Power Good						
Power Good Threshold	V_{TH_PGLH}	V_{OUT} rising (good)	88	90	92	%
Power Good Hysteresis	ΔV_{TH_PGLH}		--	15	--	%
Power Good Delay Time			--	10	--	μs
CLK Output						
CLK Output Voltage (High-Level)	V_{CLKH}	I_{VCLK} = −10mA	4.9	5	5.1	V
CLK Output Voltage (Low-Level)	V_{CLKL}	I_{VCLK} = 10mA	0	0.1	0.2	V
CLK Frequency	f_{CLK}		--	300	--	kHz
LDO Regulator						
LDO Output Voltage	V_{LDO}	V_{IN} = 12V, no load	3.267	3.3	3.333	V
		V_{IN} > 6V, I_{LDO} < 100mA	3.217	3.3	3.383	
		V_{IN} > 5.5V, I_{LDO} < 35mA	3.267	3.3	3.333	
		V_{IN} > 5V, I_{LDO} < 20mA	3.217	3.3	3.383	
LDO Output Current Limit	I_{LMTLDO}		150	200	300	mA
Bypass Switch						
Bypass Switch RON	R_{BYP}		--	3	--	Ω
Bypass Switch Turn-on Voltage	V_{BYP_ON}	RT6228A/B	--	4.7	--	V
Bypass Switch Switchover Hysteresis			--	0.2	--	V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C

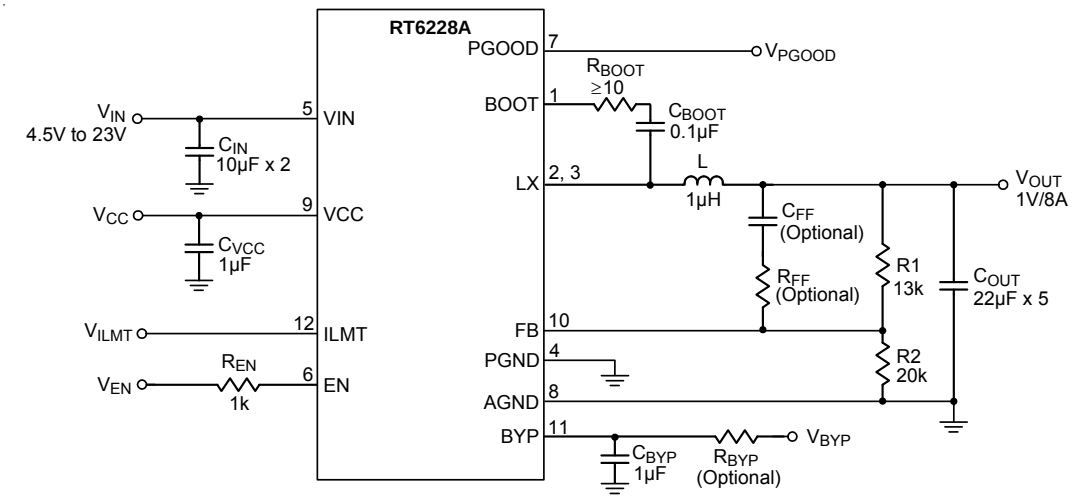
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

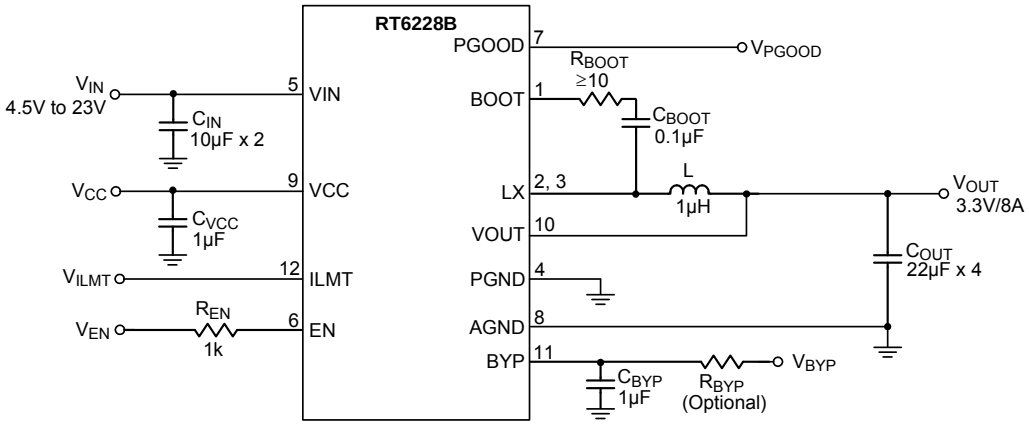
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Richtek Evaluation Board.

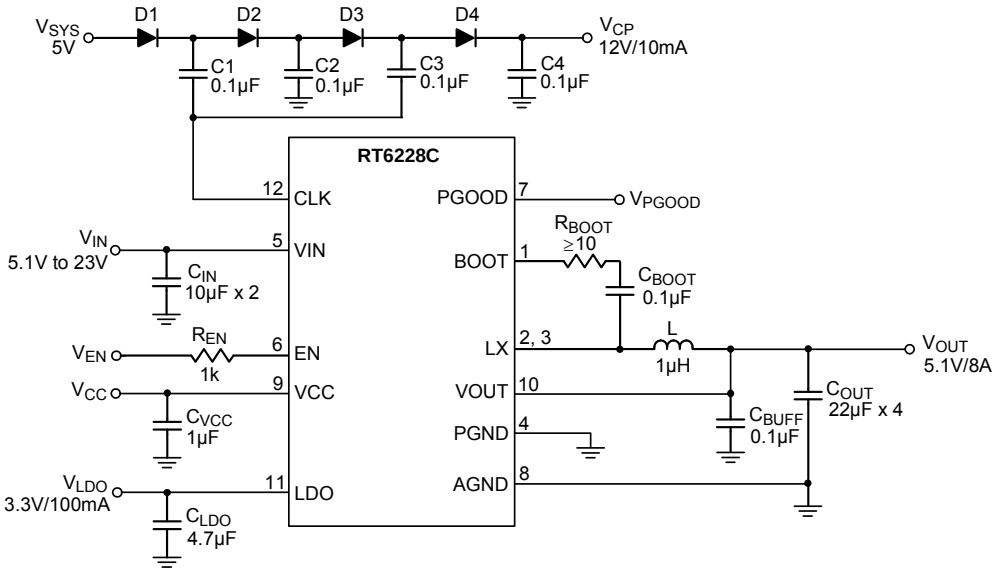
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

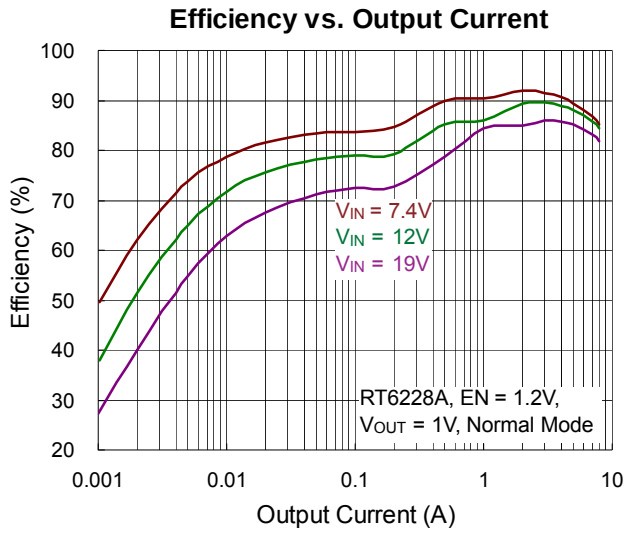
Typical Application Circuit

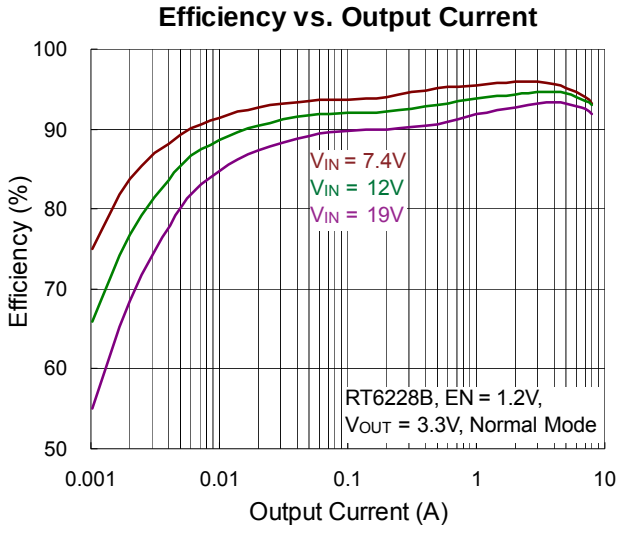


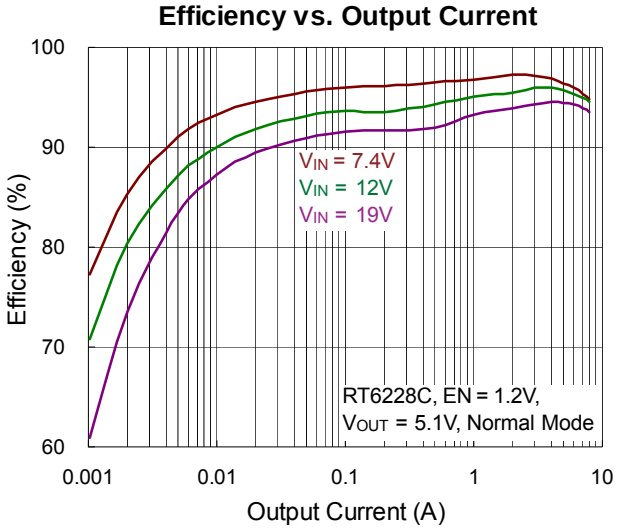


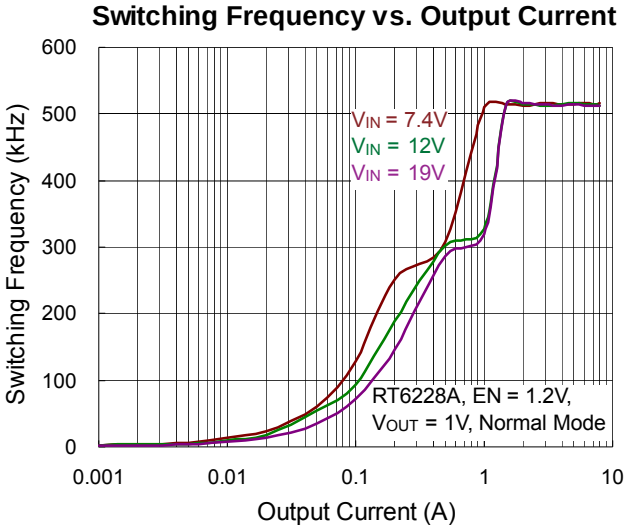


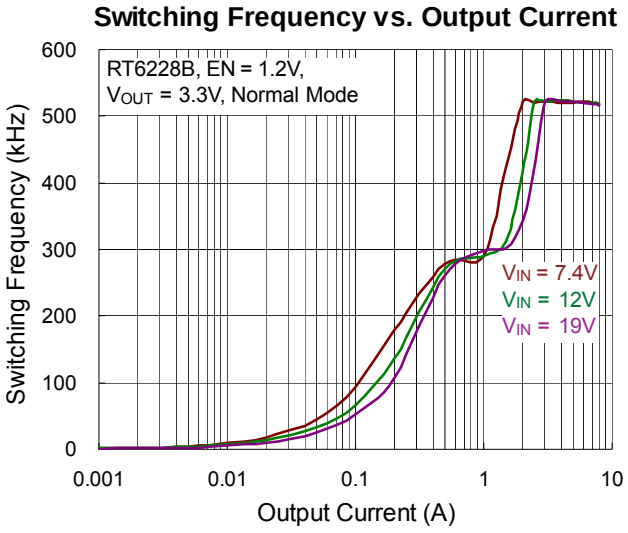
Typical Operating Characteristics

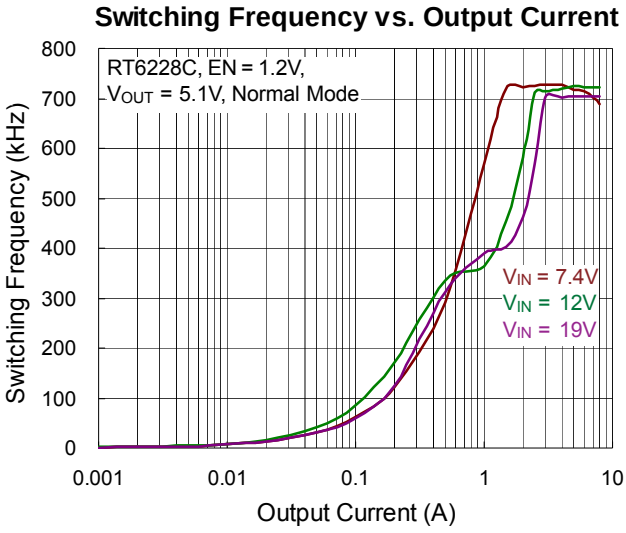




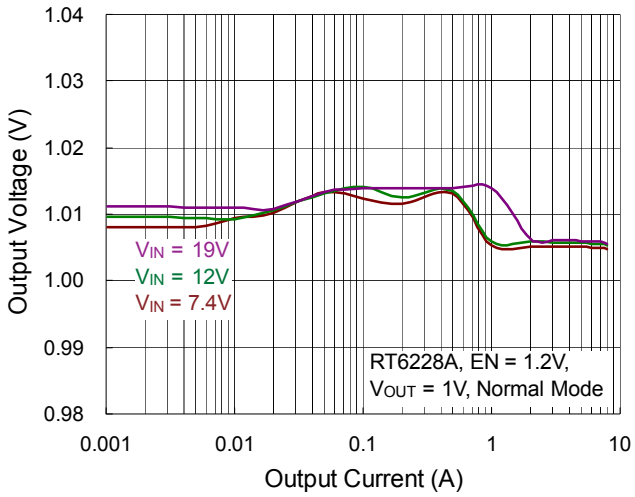








Output Voltage vs. Output Current



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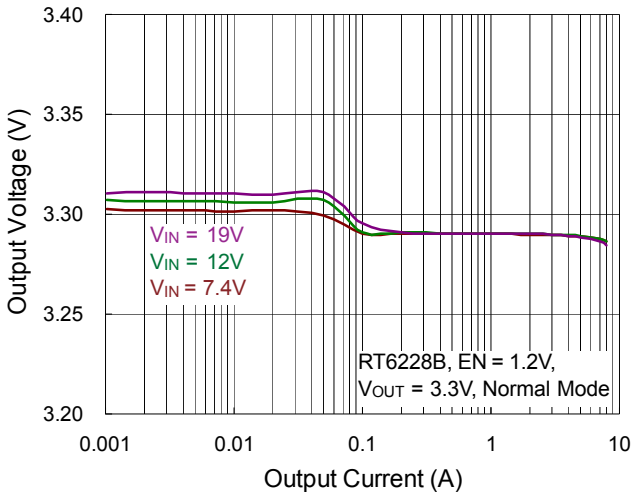
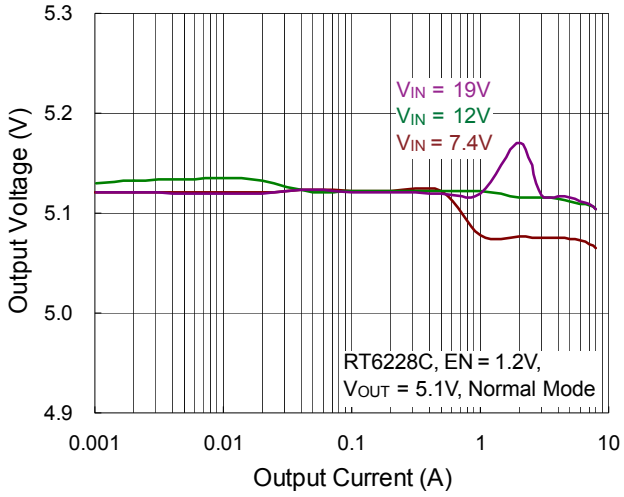
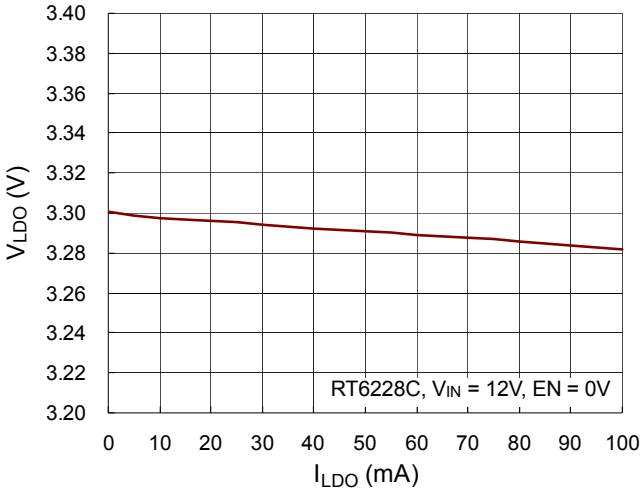


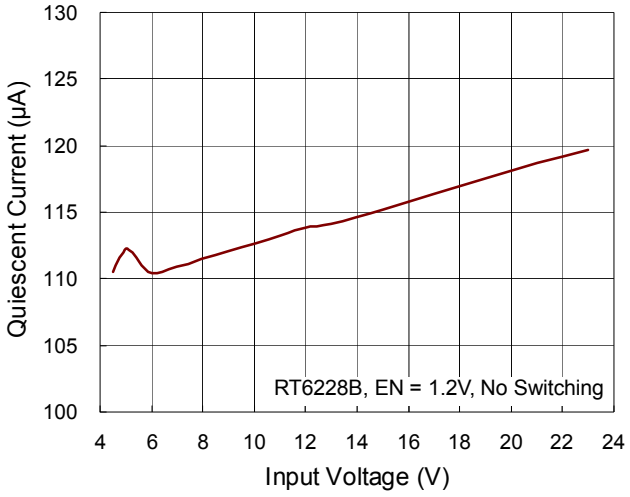
Output Voltage vs. Output Current



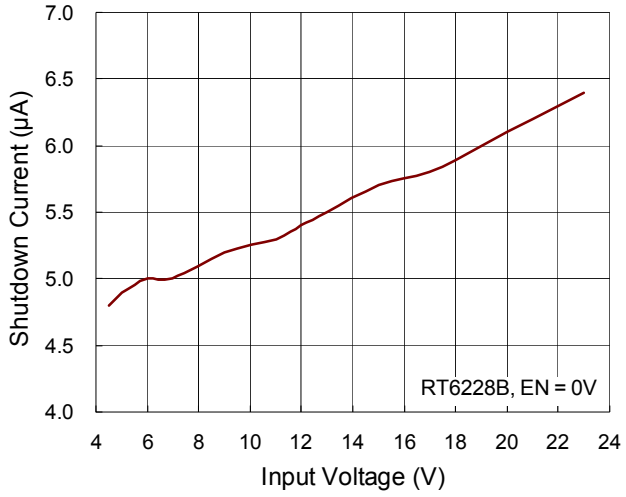
V_{LDO} vs. I_{LDO}



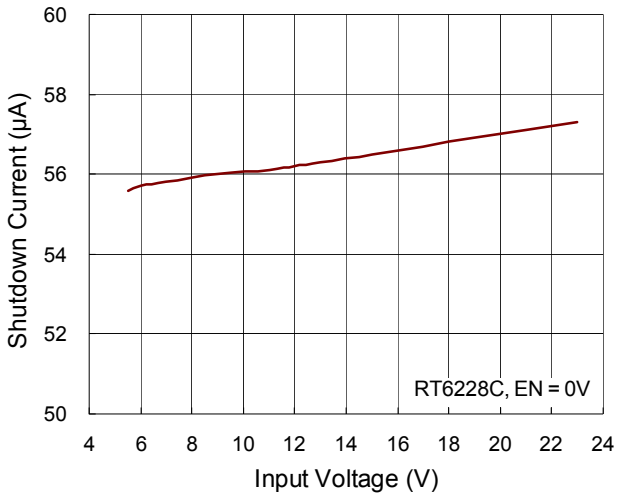
Quiescent Current vs. Input Voltage



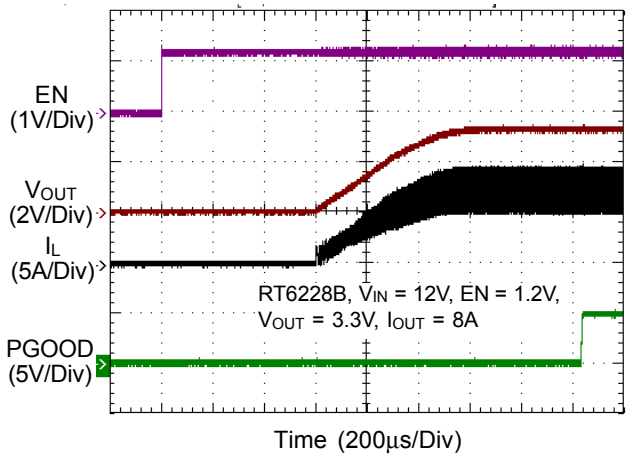
Shutdown Current vs. Input Voltage



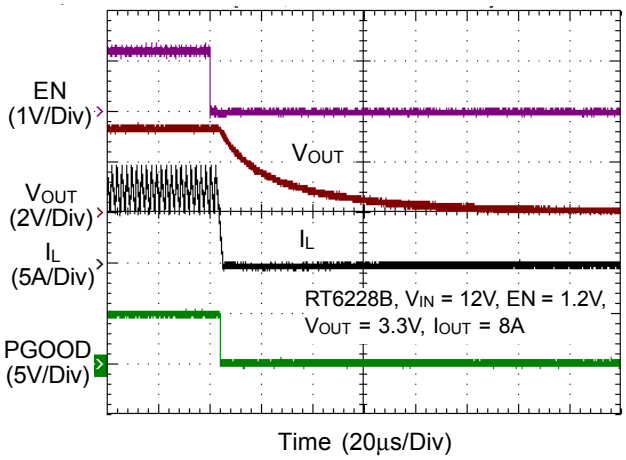
Shutdown Current vs. Input Voltage



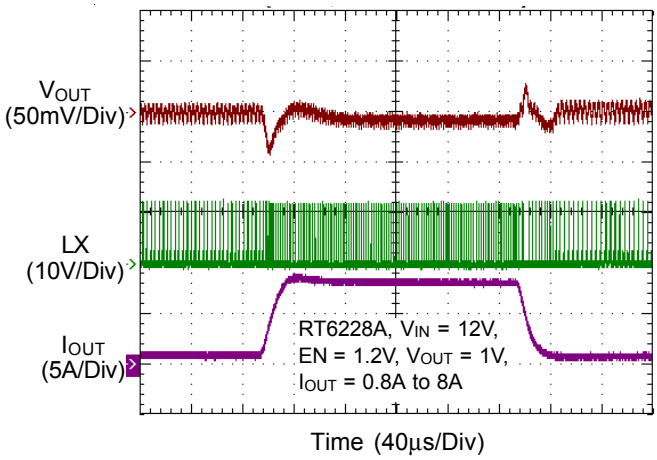
Power On from EN



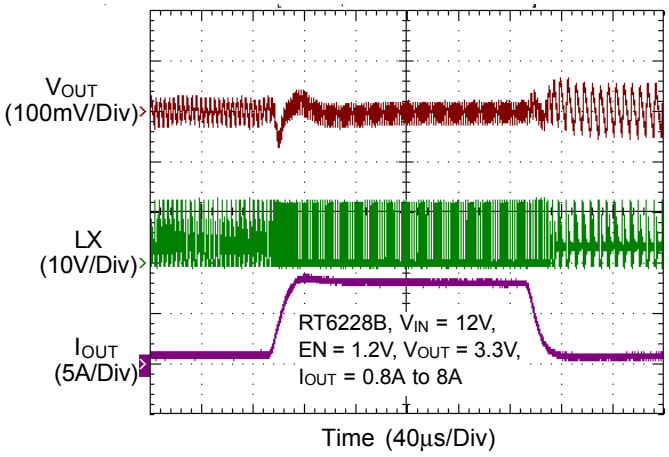
Power Off from EN



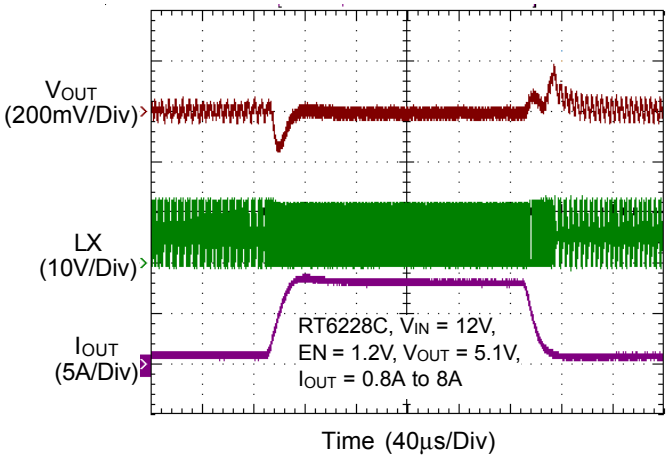
Load Transient Response



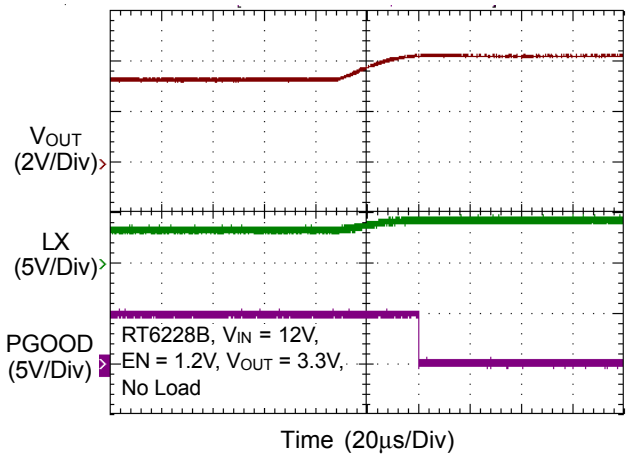
Load Transient Response



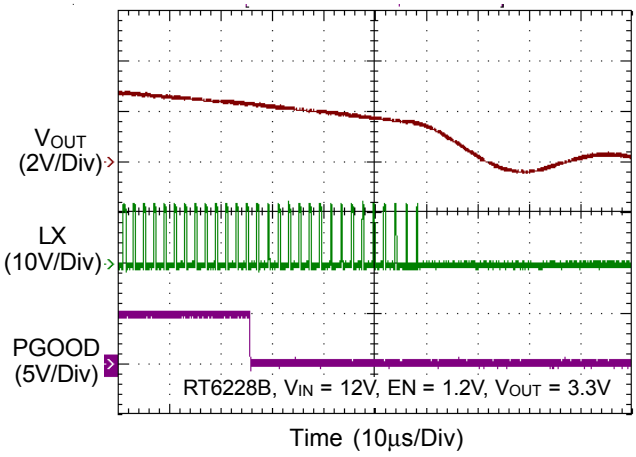
Load Transient Response



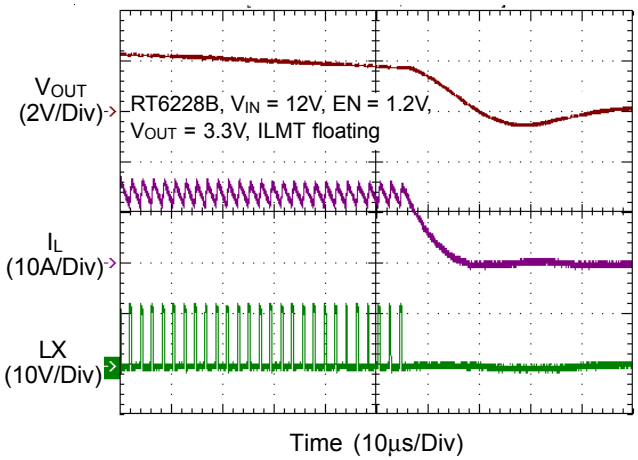
VOUT OVP



VOUT UVP



Over Current Limit



Application Information

The RT6228A/B/C is high-performance 8A step-down regulators with internal power switches and synchronous rectifiers. They feature an Advanced Constant On-Time (ACOT®) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 23V. The output voltage are fixed 3.3V (RT6228B), 5.1V (RT6228C) or adjustable from 0.6V to 5.1V (RT6228A).

The proprietary ACOT® control scheme improves conventional constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

The RT6228C includes a 3.3V linear regulator (LDO). The linear regulator provides an automatic saving power function, when VOUT rises above 4.7V, an automatic circuit will change the power source of linear regulator from VIN path to VOUT path, therefore the power dissipation of linear regulator will be decrease efficiently.

ACOT® Control Architecture

The conventional CFCOT (constant frequency constant on-time) control which making the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve good constant-frequency behavior. Because voltage drops across the MOSFET switches and inductor cause sensing mismatch as sensing input and output voltage from LX pin. When the load change, the voltage drops across the MOSFET switches and inductor cause a switching frequency variation with load current. One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT®uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT® One-Shot Operation

The RT6228A/B/C control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time,

the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot

is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (200ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Average Output Voltage Control Loop

In continuous conduction mode, the RT6228A/B/C provides a average output voltage control loop to cancel the DC error between $V_{FB(average)}$ and V_{REF} by adjusting the comparator input V_{REF} to make $V_{FB(average)}$ always follow designed value. This loop can efficiently improves the load and line regulation without affecting the transient performance. The operation figure is shown in Figure 1.

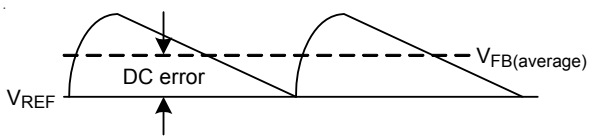


Figure 1. Average Output Voltage Control Loop Operation

High Voltage Conversion Ratio Function

Due to minimum off time limitation, the voltage conversion ratio will be limited in 2S battery application. Therefore the RT6228C provides increasing on-time function to enhance voltage conversion ratio for 2S battery application.

Diode Emulation Mode (DEM)

In diode emulation mode, the RT6228A/B/C automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 2. and can be calculated as follows :

$$I_{LOAD} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

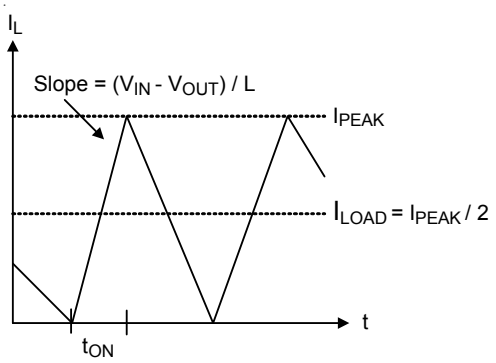


Figure 2. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

At boundary condition of discontinuous switching and continuous, the on-time is immediately increased to add "hysteresis" to discourage the IC from discontinuous switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for designed switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

Ultrasonic Mode (USM)

The RT6228A/B/C activates a unique type of diode emulation mode with a minimum switching period of 30μs (typical), called ultrasonic mode. This mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate driver signal is "OR"ed with an internal oscillator (>33kHz).

Once the internal oscillator is triggered, the controller will turn on UGATE and give it shorter on-time. When the on-time expired, LGATE turns on until the inductor current goes to zero crossing threshold and keep both high-side and low-side MOSFET off to wait for the next trigger. Because shorter on-time causes a smaller pulse of the inductor current, the controller can keep output voltage and switching frequency simultaneously. The on-time decreasing has a limitation and the output voltage will be lifted up under the slight load condition. After decreased on-time, the controller employs longer LGATE to pull down

the output voltage, which can keep output voltage at correct threshold.

Ultrasonic mode is selected by the EN voltage level. When EN is above 2.3V, it enters ultrasonic mode. If EN is in the range of 0.8V to 1.7V, it enters normal mode.

On-Time Reduction Function for DEM

In normal diode emulation mode, the output voltage ripple of converter is proportional to on-time and inversely proportional to load current. In order to have smaller voltage ripple in light load application, the RT6228A/B/C provides a smart reduction on-time function, which will follow decreased load current to decrease on-time naturally, therefore the output voltage ripple can be reduced effectively.

Linear Regulators (LDO & VCC)

The RT6228C includes a 3.3V linear regulators (LDO). The regulators can supply up to 100mA for external load, therefore it's recommended to bypass LDO with a minimum 4.7μF ceramic capacitor to GND. When VOUT is higher than the switch over threshold 4.7V, an automatic circuit will change the power source of linear regulator from VIN path to VOUT path, therefore the power dissipation of linear regulator will be decrease efficiently.

The RT6228A/B/C also includes a 5V linear regulator (VCC). The VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads.

Bypass Function for VCC (RT6228A/B)

When PGOOD is pulled high and BYP pin of RT6228A/B voltage is above 4.7V, an internal 3Ω P-MOSFET switch connects VCC to the BYP pin while the VCC linear regulator is simultaneously turned off. Because the VCC is power source for internal logic device and gate driver. If bypass function was enabled, it' s recommended to put a RC filter to BYP pin to enhance power quality for IC internal power.

VCLK for Charge Pump (RT6228C)

A 300kHz VCLK signal can be used for the external charge pump circuit. The VCLK signal becomes available when PGOOD signal pull high. VCLK driver circuit is driven by VOUT pin voltage. In order to suppress output voltage variation of converter when VCLK loaded from VOUT pin, it is recommended to bypass a minimum 0.1uF ceramic capacitor from VOUT pin to GND as close as possible. In a design that does not require VCLK output, shorted VCLK pin and GND so that VCLK is turned off.

The external 14V charge pump is driven by VCLK. As shown in Figure 3, when VCLK is low, C1 will be charged by VOUT through D1. C1 voltage is equal to VOUT minus the diode drop. When VCLK becomes high, C1 transfers the charge to C2 through D2 and charges C2 voltage to VCLK plus C1 voltage. As VCLK transitions low on the next cycle, C3 is charged form C2 voltage minus a diode drop through D3. Finally, C3 charges C4 through D4 when VCLK switches high. Thus, the total charge pump voltage, VCP is :

$$V_{CP} = V_{OUT} + 2 \times V_{CLK} - 4 \times V_D$$

where VCLK is the peak voltage of the VCLK driver which is equal to VOUT pin voltage and VD is the forward voltage dropped across the Schottky diode.

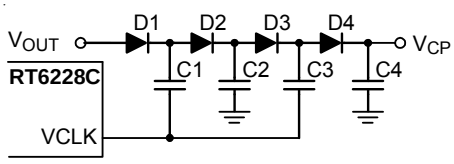


Figure 3. Charge Pump Circuit Connected to VCLK

Current Limit

The RT6228A/B/C current limit is fixed 9A (RT6228C) or adjustable (8A,10A,12A) by ILMT pin (RT6228A/B) and it is a cycle-by-cycle “valley” type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit, another on-time is permitted. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection

level (see next section) the IC will stop switching to avoid excessive heat.

Peak Current-Limit Protection

The RT6228A/B/C integrates a high-side MOSFET current limit protection for preventing inductor saturation or avoiding any possibility of damage caused by too much inrush current. For implementing peak current limit protection, there is a I_{LIMIT_PEAK} level (≈ 15A) is compared to switching current during high-side MOSFET turned on, as shown in Figure 4. As the inductor current I_L reaches the I_{LIMIT_PEAK}, the on-time is terminated to limit the load current. Further, low-side MODFET is turned on to discharge the inductor current till VOUT is lower than the internal V_{REF}. For regulating the output voltage, high-side MOSFET is turned on which is the cycle-by-cycle current limit. However, if this situation still exists and the duty cycle is suppressed, output voltage cannot be regulated and starts falling. Once, the output voltage below UVP level, RT6228A/B/C is going to be latched.

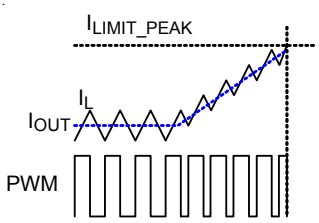


Figure 4. Peak Current Limitation

Output Over-Voltage Protection and Under-Voltage Protection

The RT6228A/B/C includes output over-voltage protection (OVP). If the output voltage rises above the regulation level, the high-side switch naturally remains off and the synchronous rectifier will turn on until the inductor current reaches the zero or next on-time one-shot is triggered. If the output voltage exceeds the OVP threshold for longer than 20μs (typical), the IC's OVP is triggered. The RT6228A/B/C also includes output under-voltage protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 20μs (typical) the IC' s UVP is triggered. The RT6228A/B/C uses latch-off mode in OVP and UVP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Input Under-Voltage Lock-Out

In addition to the enable function, the RT6228A/B/C provides an Under-Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Over-Temperature Protection

The RT6228A/B/C includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. The RT6228A/B/C uses latch-off mode in OTP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Enable and Disable

The RT6228A/B/C's EN is used to control converter, the enable voltage (EN) has a logic-low level of 0.4V. When VEN is below this level the IC enters shutdown mode When VEN exceeds its logic-high level of 0.8V the converter is fully operational. For RT6228C, the 3.3V linear regulators (LDO) is always on when VIN exceeds the UVLO threshold. See Table1 for the RT6228A/B/C power logic.

Table 1. RT6228A/B/C Power Logic

Part.	EN	VCC	VOUT	VCLK	3.3V (LDO)
RT6228A	1	1	1	X	X
	0	0	0	X	X
RT6228B	1	1	1	X	X
	0	0	0	X	X
RT6228C	1	1	1	1	1
	0	1	0	0	1

Internal Output Voltage Discharge

An internal open-drain logic output is implemented on LX pin. As operating in OVP, UVP, OTP, enable low and VIN low status, the internal discharge path is activated and the residual energy from output terminal can be released from an internal resistor(50Ω) to ground.

Soft-Start

The RT6228A/B/C provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 0.6ms. A unique PWM duty limit control that prevents output over-voltage during soft-start period is designed specifically for FB floating.

Power Good Output (PGOOD)

The power good output is an open drain output that requires a pull-up resistor. When the output voltage is 15% (typical) below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to 90% of its set voltage once more. During soft-start, PGOOD is actively held low and only allowed to be pulled high after soft-start is over and the output reaches 90% of its set voltage. There is a 10μs delay built into PGOOD circuitry to prevent false transition.

External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor and at least 10Ω resistor between BOOT pin and LX pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{LX} rises rapidly. In some cases, it is desirable to reduce EMI further, by the expense of some additional power dissipation.

Output Voltage Setting (RT6228A)

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT,\,VALLEY} = \left(1+\frac{R1}{R2}\right)\times 0.6V$$

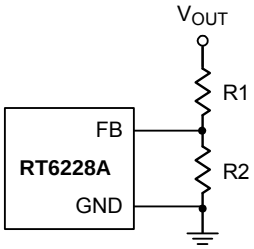


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \text{ x } (V_{OUT} - 0.6V)}{0.6V}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator.

The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The typical operating circuit is recommended to use two 10μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The IC is optimized for ceramic output capacitors and best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. However, some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increases compensations for the voltage losses. Calculate the output voltage SAG as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive SOAR is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Most applications never experience instantaneous full load steps and the IC's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that over-voltage protection and under-voltage protection will not be triggered.

Feedforward Capacitor C_{FF} Design (RT6228A)

For saving time to design compensator and reducing the layout area through external components, the components of compensator are integrated in IC. However, this integrated compensator might not suit to every load transient spec. Hence, for the RT6228A to be more adaptable, the feedforward capacitor C_{FF} is used in the feedback loop to improve transient response, as shown in Figure 6. Figure 7 shows the comparison result of bode plot with different feedback loop conditions. Referring to Figure 7, through connecting a C_{FF} in feedback network, the gain and phase are raised in mid-frequency that not only can extend the bandwidth, but boost the phase margin as well. Moreover, there is also a high frequency pole to eliminate high frequency noise. Consequently, those features of feedforward feedback network allow the RT6228A have faster response to handle different load transient.

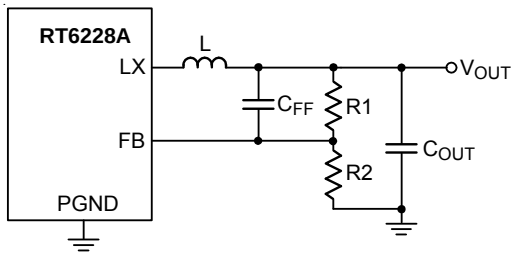


Figure 6. Feedback Loop with feedforward Capacitor.

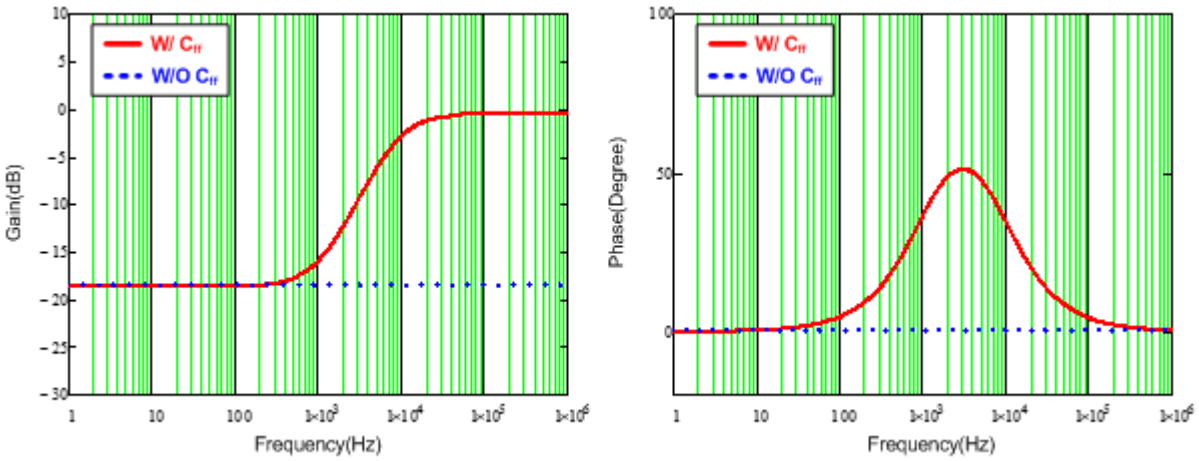


Figure 7. Bode Plot with Different Feedback Loop Conditions

The transfer function of feedforward network is expressed in equation (1) and the positions of zero and pole are calculated in equation (2) and (3).

$$\frac{V_{FB}(s)}{V_{OUT}(s)} = \frac{1}{1+\frac{R1}{R2}} \times \frac{1+\frac{s}{\frac{1}{R1\times C_{FF}}}}{1+\frac{s}{\frac{1}{(R1//R2)\times C_{FF}}}} \quad (1)$$

$$f_P = \frac{1}{2\pi\times(R1//R2)\times C_{FF}} \quad (2)$$

$$f_Z = \frac{1}{2\pi\times R1\times C_{FF}} \quad (3)$$

Observing Figure 7, the maximum phase boost occurs between zero and pole frequencies that is defined as maximum phase boost frequency, as expressed in equation (4). Hence, in order to achieve the maximum phase boost by adding C_{FF} in the RT6228A, the system's original bandwidth has to be located at maximum phase boost frequency.

$$f_{ph\_max} = \sqrt{f_P \times f_Z} \quad (4)$$

For putting zero at the correct frequency to implement maximum phase boost, the first thing is to determine system's bandwidth. There is a simple way to measure bandwidth of the RT6228A that is load transient analysis. By using a converter without feedforward network to observe the voltage deviation frequency during load step, the bandwidth of converter can be obtained because of the crossover frequency related to voltage deviation frequency approximately, as shown in Figure 8.

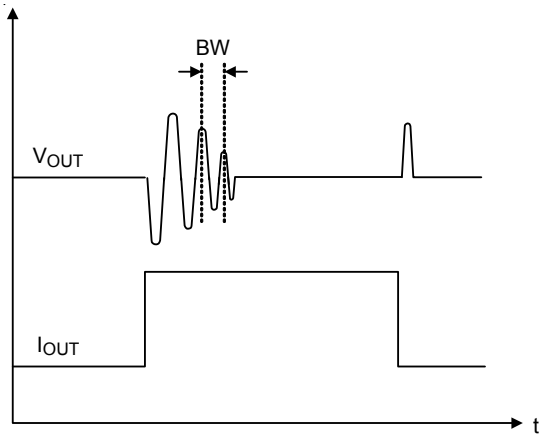


Figure 8. A Simply Way to Get the Bandwidth

Following the above concept, the equation of bandwidth with feedforward C_{FF} can be derived, as expressed in equation (5).

$$BW = \sqrt{\frac{1}{2\pi\times R1C_{FF}} \times \frac{1}{2\pi\times C_{FF}}\left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (5)$$

For optimizing transient response, the C_{FF} can be obtained from equation (5), as shown in equation (6).

$$C_{FF} = \frac{1}{2\pi\times BW}\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (6)$$

After defining the C_{FF}, please also check the load regulation, because feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over spec caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF}.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-12HL 3x3 (FC) package, the thermal resistance, θ_{JA}, is 35.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (35.8°C/W) = 2.79W for a UQFN-12HL 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

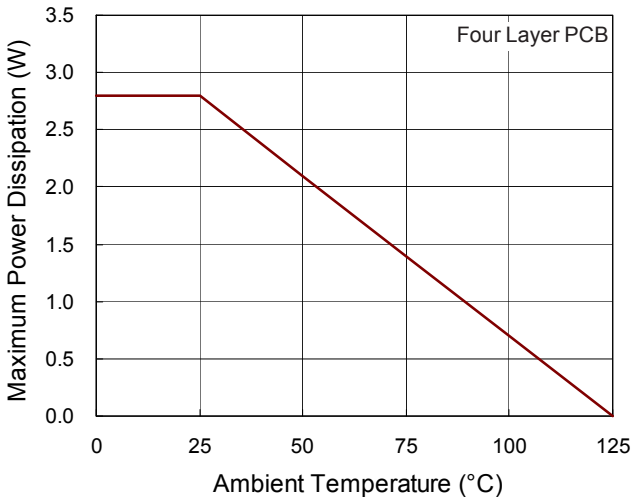


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

Printed circuit board (PCB) layout design for switch-mode power supply IC is critical and important. Improper PCB layout brings lots of misbehaviors on power supply, such as poor output voltage regulation, switching jitter, bad thermal performance, excessively radiate noise and alleviating component reliability. For avoiding those issues, designers have to understand current trace and signal flow in the switching power supply. The following design concepts present design consideration of PCB layout for switching power supply.

- For suppressing phase ring and extra power losses that affect device reliability, the input capacitor has to place close to VIN pin to reduce the influence of parasitic inductor.
- For thermal stress and power consumption considerations, the current paths of VIN and VOUT are as short and wide as possible to decrease the trace impedance.
- Since the LX node voltage swings from VIN to GND with very fast rising and falling times, switching power supply suffers quite serious EMI issues. To eliminate EMI problems, the inductor must put as close as possible to IC to narrow the LX node area. Besides, the LX node should arrange in the same plate to reduce coupling noise path caused by parasitic capacitance.

- For system stability and coupling noise elimination, the sensitive components and signals, such as control signal and feedback loop, should keep away from LX node.
- For enhancing noise immunity on VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to IC.
- The feedback signal path from VOUT to IC should be wide and kept away from high switching path.
- The trace width and numbers of via should be based on application current to design. Make sure the switching power supply has great thermal performance and good efficiency.

An example of PCB layout guides are shown in Figure 10 to Figure 12 for reference.

RT6228A

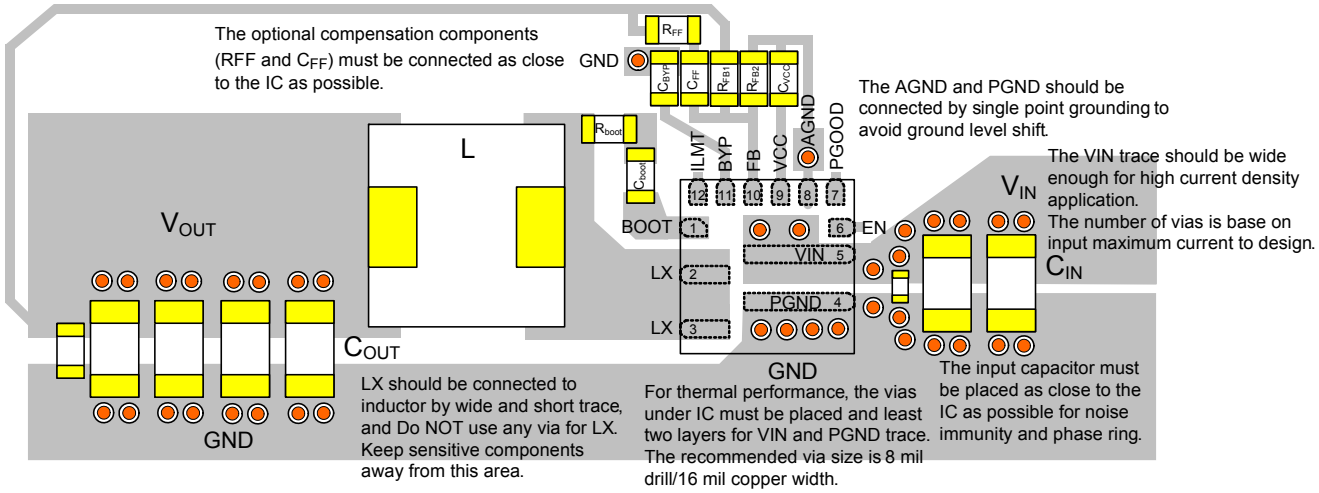


Figure 10. Layout Guide of RT6228A.

RT6228B

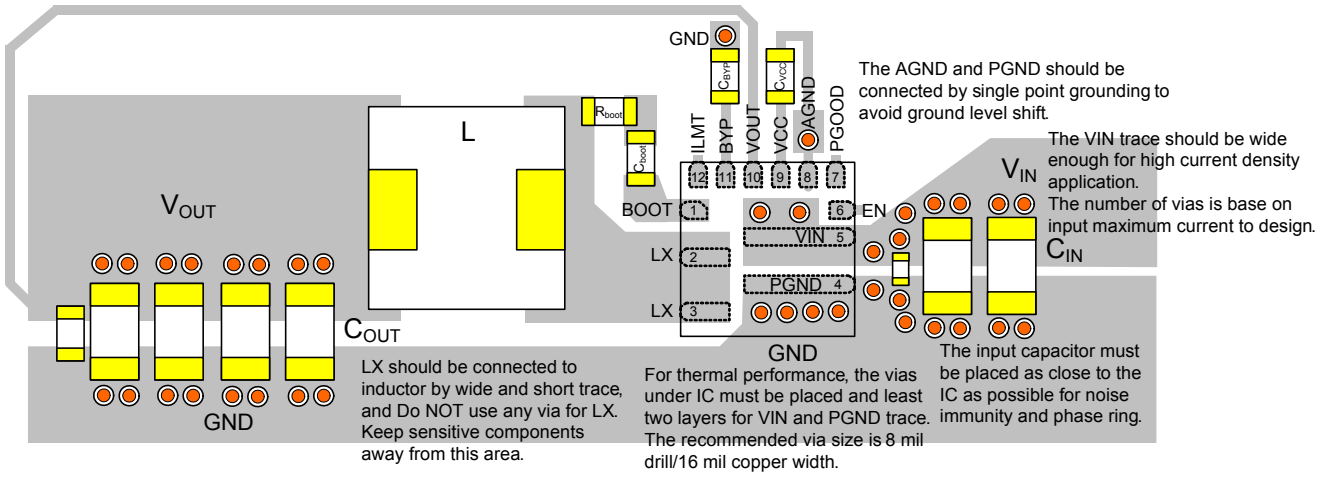


Figure 11. Layout guide of RT6228B.

RT6228C

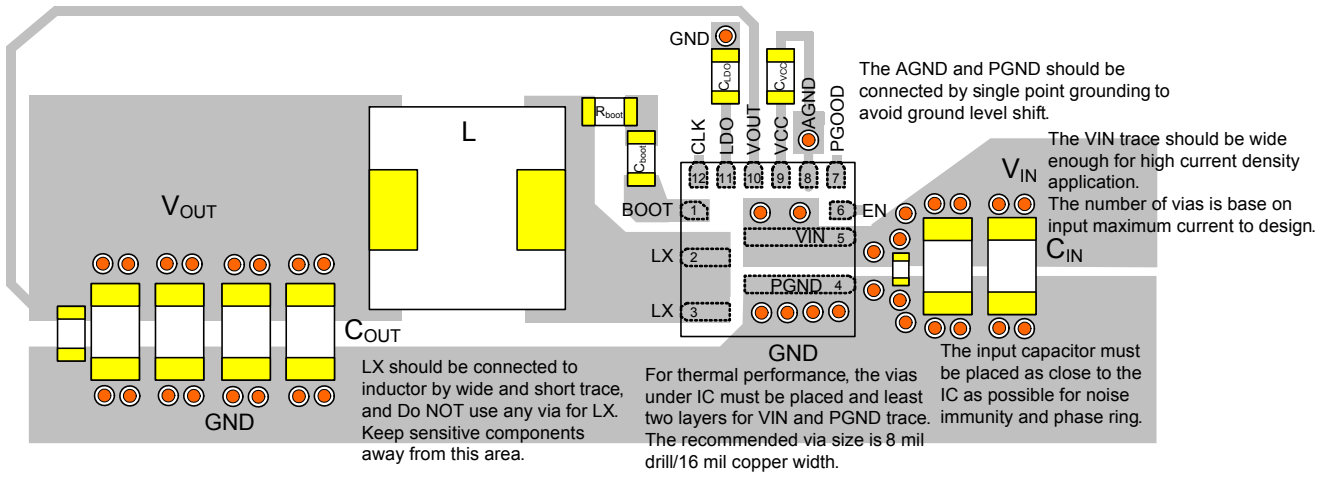


Figure 12. Layout guide of RT6228C.

Trace Width Design

For thermal, efficiency and PCB handling current capability, the trace width design is very important. According to IPC-2221 formally IDC-D-275 PWB, the following formulas can be used to calculate the trace width for printed circuit boards.

Inner trace :

$$I(Amp) = 0.015 \times \Delta T(°C)^{0.5453} \times Area(mils^2)^{0.7349}$$

Outer trace :

$$I(Amp) = 0.0647 \times \Delta T(°C)^{0.4281} \times Area(mils^2)^{0.6732}$$

$$Width(mil) = \frac{Area(mils^2)}{Thickness(oz) \times 1.37\left(\frac{mil}{oz}\right)}$$

where

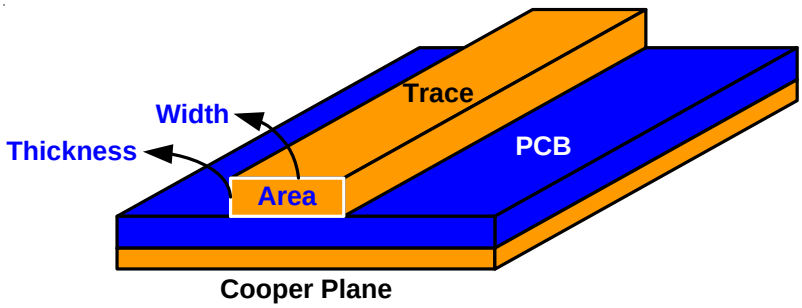
I(Amp) = Current,

$\Delta T(°C)$ = Temperature rise,

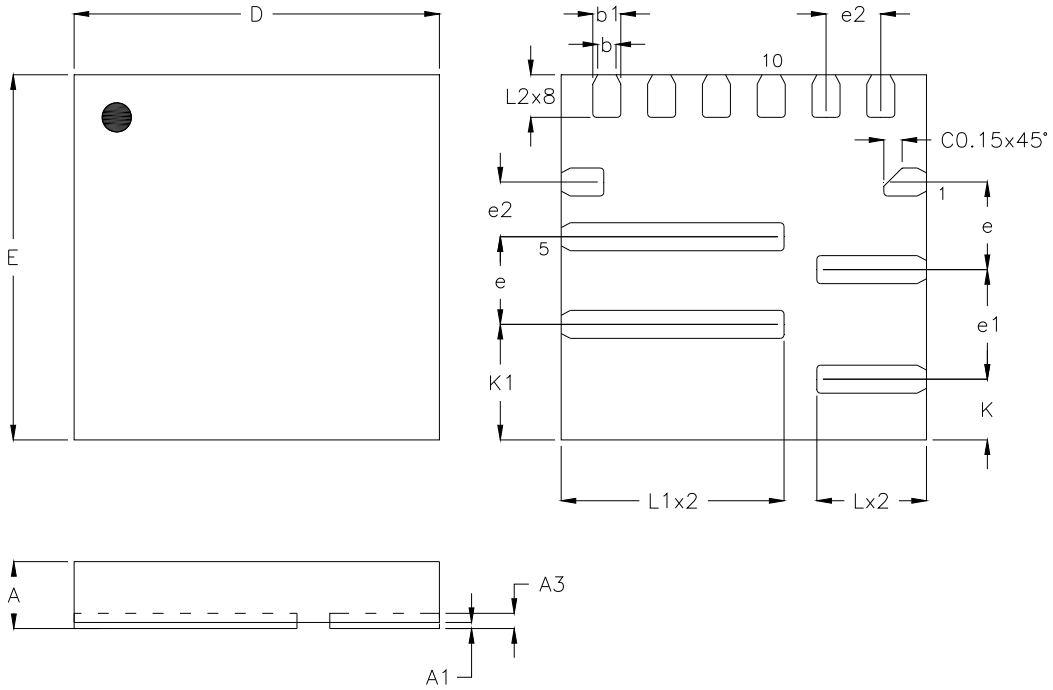
$Area(mils^2)$ = Cross sectional area = Width x Thickness,

Width(mil) = Trace width, and

Thickness(oz) = Layer Cu thickness.



Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.100	0.200	0.004	0.008
b1	0.180	0.280	0.007	0.011
L	0.800	1.000	0.031	0.039
L1	1.730	1.930	0.068	0.076
L2	0.250	0.450	0.010	0.018
e	0.720		0.028	
e1	0.900		0.035	
e2	0.450		0.018	
K	0.500		0.020	
K1	0.950		0.037	

U-Type 12HL QFN 3x3 (FC) Package

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