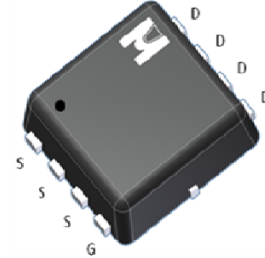
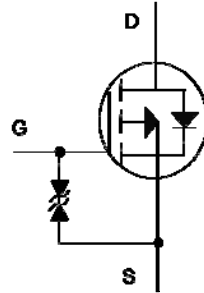


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on)}$ (MAX.)	8.5m Ω
I_D	-25A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-20	A
	$T_C = 100\text{ }^\circ\text{C}$		-18	
Pulsed Drain Current ¹		I_{DM}	-100	
Avalanche Current		I_{AS}	-25	
Avalanche Energy	$L = 0.1\text{mH}, I_D = -25\text{A}, R_G = 25\text{ }\Omega$	E_{AS}	31.25	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	2.5	W
	$T_C = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = -15\text{V}$, $L = 0.1\text{mH}$, $V_G = -10\text{V}$, $I_L = -20\text{A}$, Rated $V_{DS} = -30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	μA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-25			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -10V, I _D = -12A		7	8.5	mΩ
		V _{GS} = -4.5V, I _D = -9A		12	15	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -12A		26		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		3091		pF
Output Capacitance	C _{oss}			476		
Reverse Transfer Capacitance	C _{rss}			404		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.5		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -12A		54		nC
	Q _g (V _{GS} =4.5V)			32		
Gate-Source Charge ^{1,2}	Q _{gs}			7.3		
Gate-Drain Charge ^{1,2}	Q _{gd}			13		
Turn-On Delay Time ^{1,2}	t _{d(on)}		V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 2.7Ω		24	
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			70		
Fall Time ^{1,2}	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-25	A
Pulsed Current ³	I _{SM}				-100	
Forward Voltage ¹	V _{SD}	I _F = -12A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		52		nS
Reverse Recovery Charge	Q _{rr}			60		nC

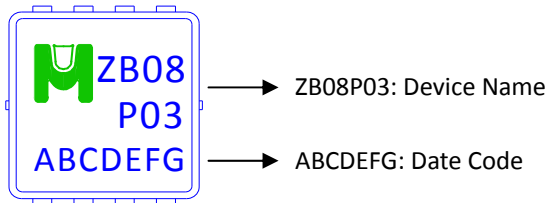
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

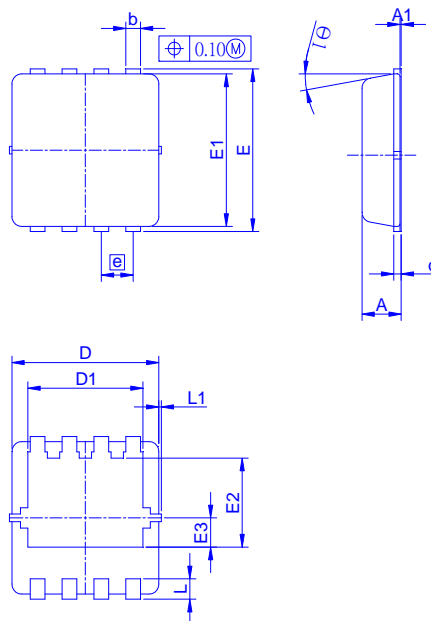
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZB08P03V for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads

