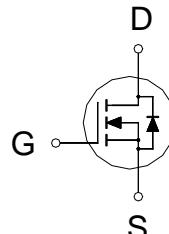


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DSON} (MAX.)	20mΩ
I _D	12A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	12	A
	T _C = 100 °C		9	
Pulsed Drain Current ¹		I _{DM}	48	
Avalanche Current		I _{AS}	8	
Avalanche Energy	L = 0.1mH, ID=8A, RG=25Ω	E _{AS}	3.2	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	1.6	
Power Dissipation	T _C = 25 °C	P _D	21	W
	T _C = 100 °C		8.3	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	6	50	°C / W
Junction-to-Ambient ³	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	12			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 8A$		15.5	20	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 6A$		25	30	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 8A$		16		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		520		pF
Output Capacitance	C_{oss}			88		
Reverse Transfer Capacitance	C_{rss}			62		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		2.0		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 8A$		11.5		nC
	$Q_g(V_{GS}=4.5V)$			5		
Gate-Source Charge ^{1,2}	Q_{gs}			1.6		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.8		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		9		nS
Rise Time ^{1,2}	t_r			12		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			30		
Fall Time ^{1,2}	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{GS} = 0V$			2.3	A
Pulsed Current ³	I_{SM}				9.2	
Forward Voltage ¹	V_{SD}				1.2	
Reverse Recovery Time	t_{rr}			45		
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			30		
Reverse Recovery Charge	Q_{rr}			2		

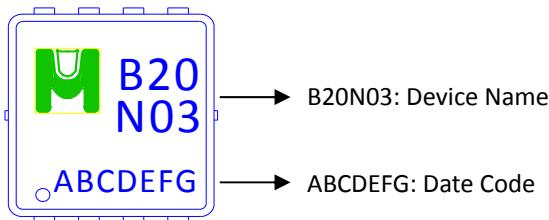
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

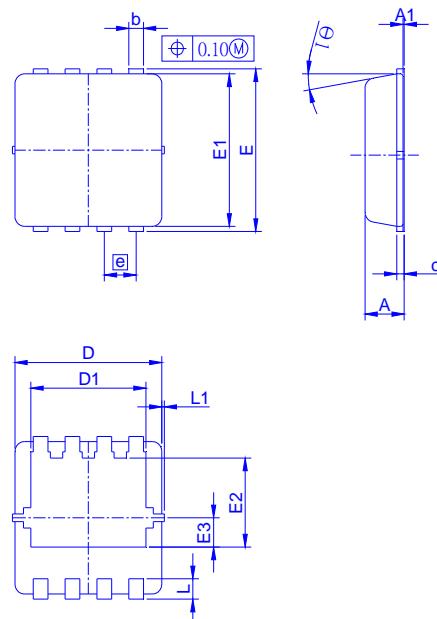
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB20N03V for EDFN 3 x 3



Outline Drawing



Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	θ_1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads

