March 2006

FAN7314
LCD Backlight Inverter Drive IC

Features

- High-efficiency single-stage power conversion
- Wide input voltage range: 5V to 25.5V
- Back light lamp ballast and soft dimming
- Reduces number of required external components
- Precision voltage reference trimmed to 2%
- ZVS half-bridge topology
- Soft start
- PWM control at fixed frequency
- Analog and burst dimming function
- Programmable striking frequency
- Open lamp protection
- Open lamp regulation
- 20-Pin SOIC

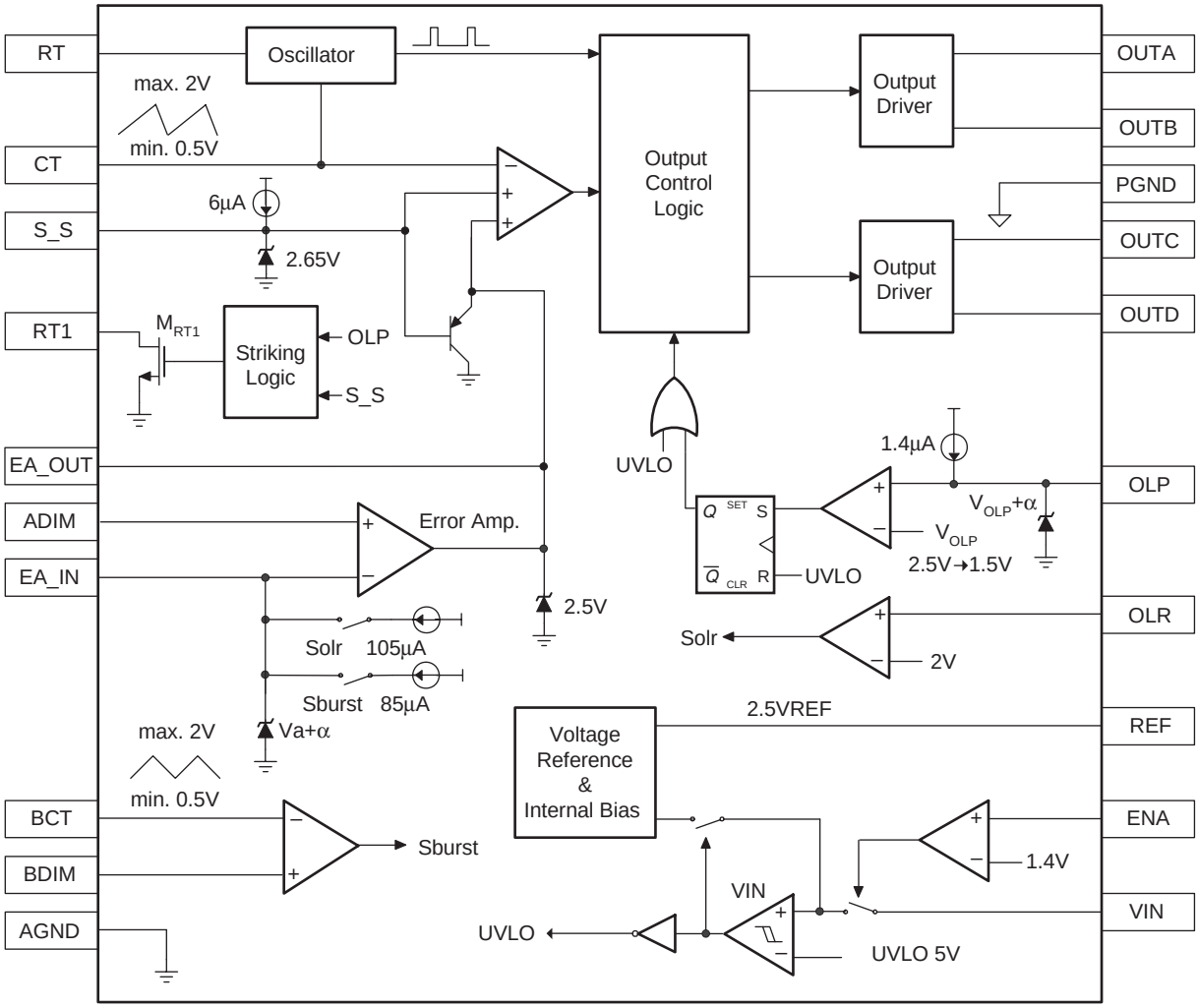
Description

The FAN7314 provides all the control functions for use as a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the CCFL and the transformer's characteristics.

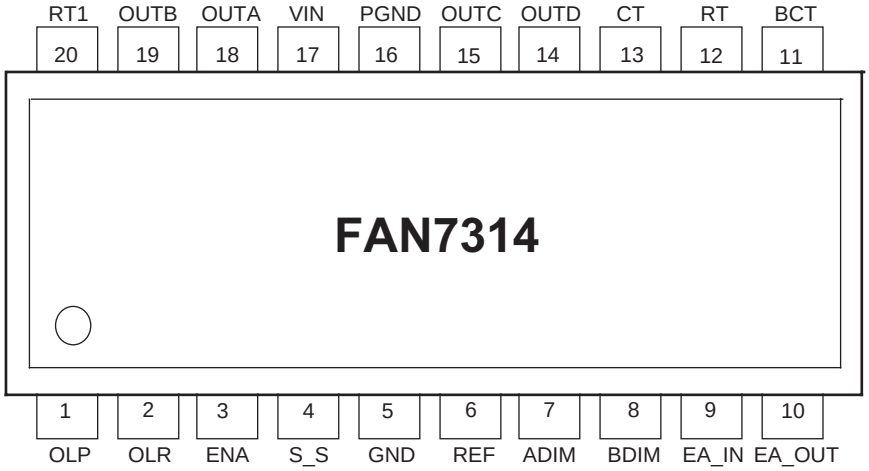
Ordering Information

Product number	Package	Operating Temperature
FAN7314M	20-SOIC	-25°C to 85°C
FAN7314MX		

Internal Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	OLP	Open Lamp Protection
2	OLR	Open Lamp Regulation
3	ENA	Enable Input
4	S_S	Soft Start
5	GND	Analog Ground
6	REF	2.5V Reference Voltage
7	ADIM	Analog Dimming Input
8	BDIM	Burst Dimming Input
9	EA_IN	Error Amplifier Input
10	EA_OUT	Error Amplifier Output
11	BCT	Burst Dimming Timing Capacitor
12	RT	Timing Resistor
13	CT	Timing Capacitor
14	OUTD	NMOSFET Drive Output D
15	OUTC	PMOSFET Drive Output C
16	PGND	Power Ground
17	VIN	Supply Voltage
18	OUTA	PMOSFET Drive Output A
19	OUTB	NMOSFET Drive Output B
20	RT1	Striking Frequency Resistor

Absolute Maximum Ratings

For typical values T_A = 25°C, V_{CC} = 12V and for min/max values T_A is the operating ambient temperature range with –25°C ≤ T_A ≤ 85°C and 5V ≤ V_{CC} ≤ 25.5V, unless otherwise specified.

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	5 to 25.5	V
Topr	Operating Temperature Range	-25 to 85	°C
Tj	Junction Temperature	150	°C
Tstg	Storage Temperature Range	-65 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Air(1, 2)	70	°C/W
Pd	Power Dissipation	1.8	W

Notes:

1. Thermal resistance test board:
   Size: 76.2mm x 114.3mm x 1.6mm(1S0P)
   JEDEC standard: JESD51-2, JESD51-3
2. Assume no ambient airflow.

ESD Level

Parameter	Pins	Conditions	Level	Unit
Human Body Model (HBM)	All pins	R = 1.5kΩ, C = 100pF	2000	V
Machine Model (MM)	All pins except for BDIM	C = 200pF	300	
	BDIM		250	

Electrical Characteristics

For typical values T_A = 25°C, V_{CC} = 12V and for min/max values T_A is the operating ambient temperature range with –25°C ≤ T_A ≤ 85°C and 5V ≤ V_{CC} ≤ 25.5V, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION (Recommend X7R Capacitor)						
ΔVref	Line Regulation	5 ≤ V_{CC} ≤ 25.5V	–	2	25	mV
V25	2.5V Regulation Voltage		2.45	2.5	2.55	V
OSCILLATOR SECTION (Main)						
fosc	Oscillation Frequency	T_A = 25°C, Ct = 270pF Rt = 18k	110.4	115	119.6	kHz
		Ct = 270pF, Rt = 18k	108	115	122	
Vcth	CT High Voltage		–	2.0	–	V
Vctl	CT Low Voltage		–	0.5	–	V
OSCILLATOR SECTION (Burst)						
foscb	Oscillation Frequency	T_A = 25°C, Ctb = 10nF, Rt = 18k	204.75	225	245.25	Hz
		Ctb = 10nF, Rt = 18k	201	225	248	
Vbcth	BCT High Voltage		–	2	–	V
Vbctl	BCT Low Voltage		–	0.5	–	V

Electrical Characteristics (Continued)

For typical values T_A = 25°C, V_{CC} = 12V and for min/max values T_A is the operating ambient temperature range with –25°C ≤ T_A ≤ 85°C and 5V ≤ V_{CC} ≤ 25.5V, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
ERROR AMP SECTION						
	Open Loop Gain(1)		–	80	–	dB
	Unit Gain Bandwidth(1)		–	1.5	–	MHz
Veh	Feedback Output High Voltage	EA_IN = 0V	2.13	2.4	2.57	V
Isin	Output Sink Current	EA_OUT = 1.5V	–	–	-1	mA
Isur	Output Source Current	EA_OUT = 1.5V	1	–	–	mA
Iolr	EA_IN Driving Current On OLR		75	105	135	µA
Iburst	EA_IN Driving Current On Burst Dimming		61	85	109	µA
Vfbh	Feedback High Voltage On Burst Dimming	R(EA_IN) = 60kΩ	Va + 0.1	Va + 0.4	Va + 0.7	V
SOFT START SECTION						
I_{SS}	Soft Start Current	S_S = 2V	4	6	8	µA
Vssh	Soft Start Clamping Voltage		2.3	2.65	3	V
PROTECTION SECTION						
Volp0	Open Lamp Protection Voltage 0	Start at open lamp	2.2	2.5	2.8	V
Volp1	Open Lamp Protection Voltage 1	Normal → open lamp	1.3	1.5	1.7	V
Volr	Open Lamp Regulation Voltage		1.75	2	2.25	V
Iolp	Open Lamp Protection Charging Current		0.7	1.4	2.1	µA
UNDER VOLTAGE LOCK OUT SECTION						
Vth	Start Threshold Voltage		–	–	5	V
Ist	Start Up Current	V_{CC} = Vth–0.2	–	130	180	µA
Iop	Operating Supply Current	V_{CC} = 12V	–	1.5	4	mA
Isb	Stand-by Current	V_{CC} = 12V	–	200	370	µA
ON/OFF SECTION						
Von	On State Input Voltage		2	–	5	V
Voff	Off Stage Input Voltage		–	–	0.7	V
OUTPUT SECTION						
Vpdhv	PMOS Gate High Voltage	V_{CC} = 12V	–	Vcc	–	V
Vphlv	PMOS Gate Low Voltage	V_{CC} = 12V	Vcc–10.5	Vcc–8.5	Vcc–6.5	V
Vndhv	NMOS Gate Drive Voltage	V_{CC} = 12V	6.5	8.5	10.5	V
Vndhv	NMOS Gate Drive Voltage	V_{CC} = 12V	–	0	–	V
Vpuv	PMOS Gate Voltage With UVLO Activated	V_{CC} = Vth–0.2	Vcc–0.3	–	–	V
Vnuv	NMOS Gate Voltage With UVLO Activated	V_{CC} = Vth–0.2	–	–	0.3	V
Tr	Rising Time(1)	V_{CC} = 12V, Cload = 2nF	–	200	500	ns
Tf	Falling Time(1)	V_{CC} = 12V, Cload = 2nF	–	200	500	ns

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
MAX./MIN. OVERLAP						
	Min. Overlap Between Diagonal Switches(1)	fosc = 100kHz	–	0	–	%
	Max. Overlap Between Diagonal Switches(1)	fosc = 100kHz	–	100	–	%
DELAY TIME						
	PDR_A/NDR_B(1)	Rt = 18k	–	450	–	ns
	PDR_C/NDR_D(1)	Rt = 18k	–	450	–	ns

Notes:

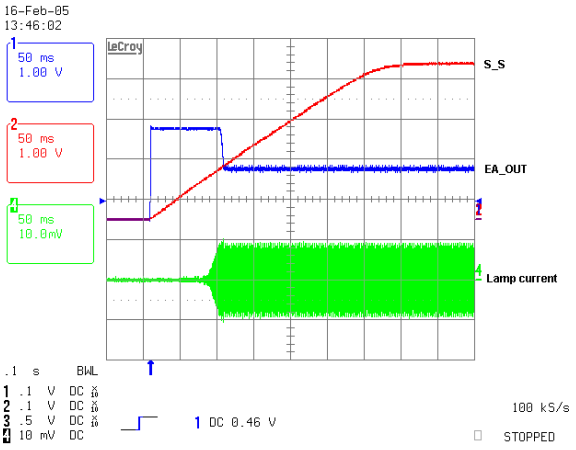
1. These parameters, although guranteed, are not 100% tesed in production.
2. Specifications to -25°C to 85°C are guaranteed by design based on final characterization results.

Function Description

UVLO: The under voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting operation as a function of the Vin value. The UVLO circuit turns on the control circuit when Vin exceeds 5V. When Vin is lower than 5V, the IC's standby current is less than 200µA.

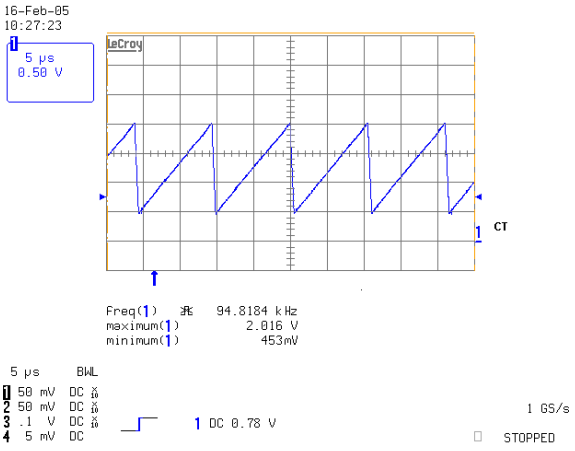
ENA: Applying voltage higher than 2V to the ENA pin enables the operation of the IC. Applying voltage lower than 0.7V to the ENA pin will disable the operation of the inverter.

Soft start: The soft start function requires that the S_S pin is connected through a capacitor to GND. A soft start circuit ensures a gradual increase in the input and output power. The capacitor value connected to the S_S pin determines the rate at which the duty ratio rises. It is charged by a 6µA current source.



Main oscillator: The timing capacitors (CTs) are charged by the reference current source. The current source is formed by the timing resistor (R_T). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform (see top of next column) charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the R_T and C_T values. The main frequency can be calculated as shown below:

$$f_{op} = \frac{19}{32\ R_T\ C_T}$$

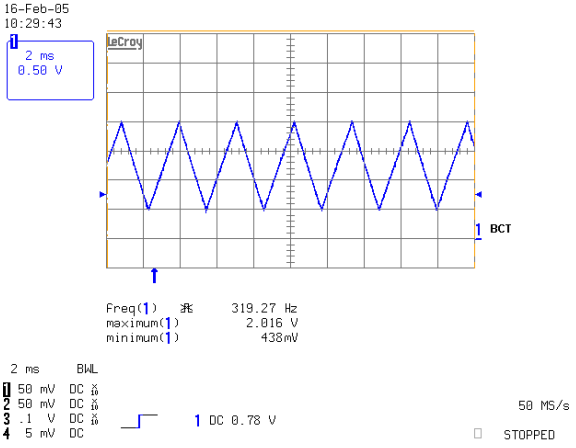


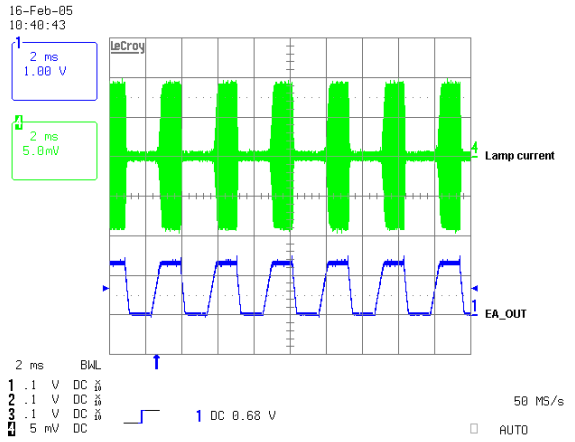
Burst oscillator & burst dimming: The timing capacitors (BCTs) are charged by the reference current source, which is formed by the timing resistor (R_T). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next the timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the R_T and BC_T values. The burst dimming frequency can be calculated as shown below:

$$f_{burst} = \frac{3.75}{96\ R_T\ BC_T}$$

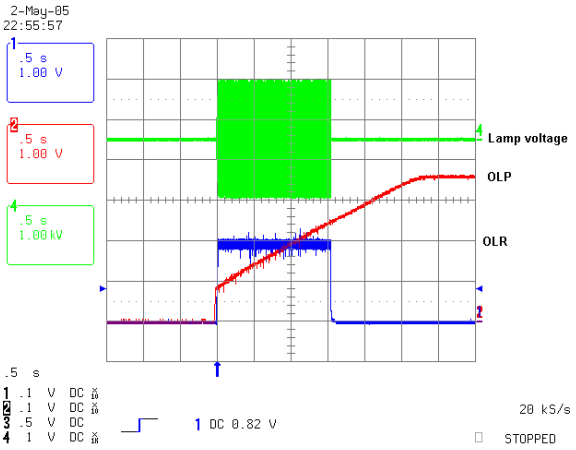
To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

By comparing the input of BDIM pin with the 0.5 to 2V triangular wave of the burst oscillator, the PWM pulses for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85µA into the EA_IN pin.





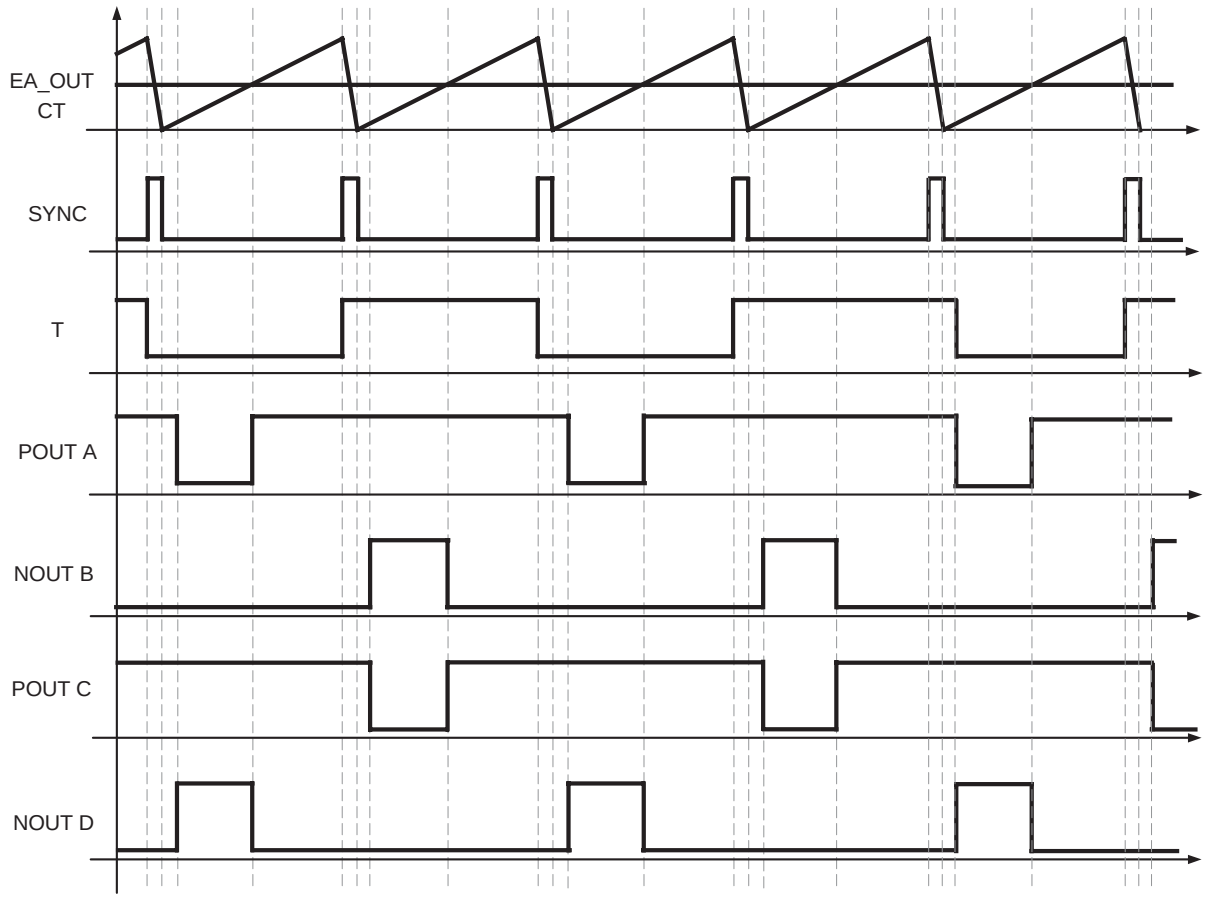
Open lamp regulation & open lamp protection: It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters regulation mode and controls the EA_OUT voltage. This limits the lamp voltage by summing 105µA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4µA internal current source. Once it reaches 2.5V, the IC enters shut down where all the output is high.



Output Drives: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair will drive the other half-bridge.

Timing Diagram

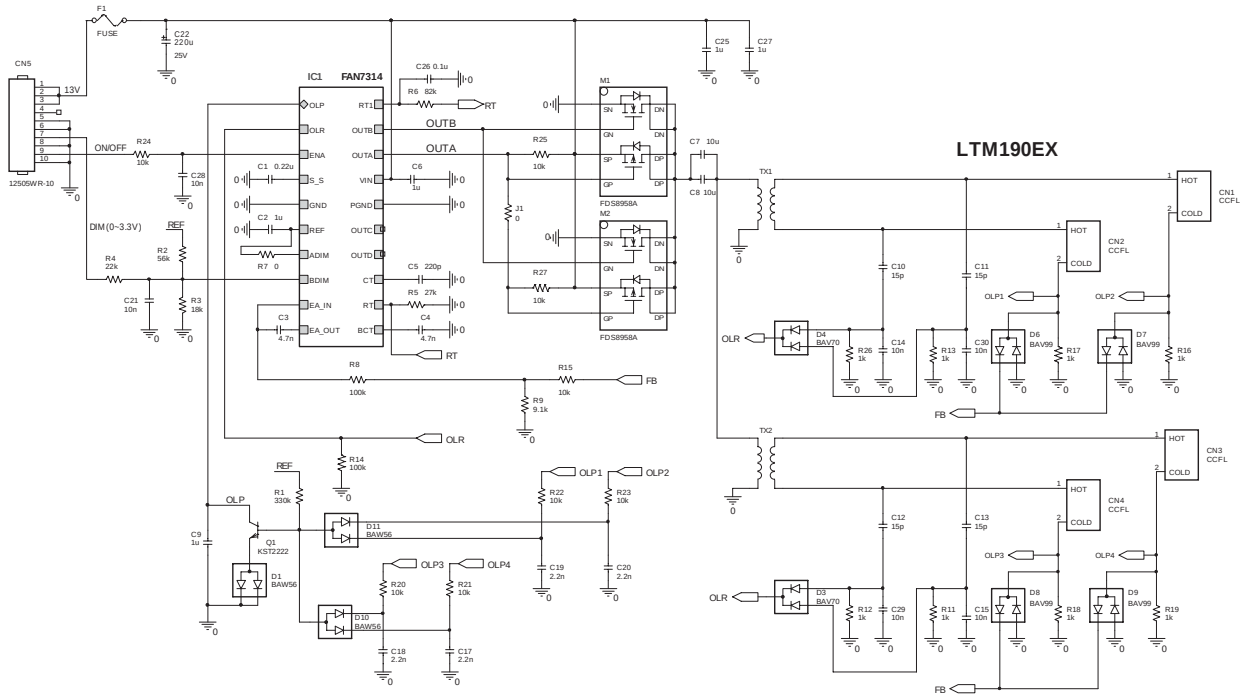
The FAN7314 uses the half-bridge to drive CCFL.



Typical Application Circuit

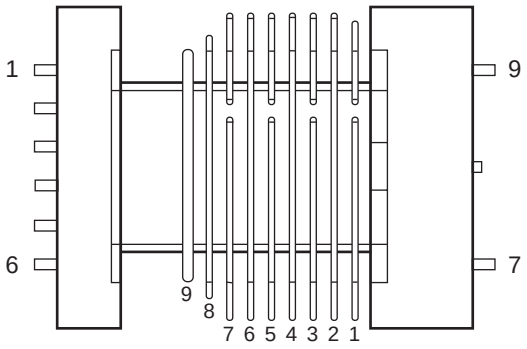
Application	Lamps	Input Voltage
19 inch LCD Monitor	4	13V

1. Schematic



2. Transformer Schematic Diagram

Supported by Namyang electronics (http://www.namyangelec.co.kr)



3. Core & Bobbin

- Core: EFD2124
- Material: PL7
- Bobbin: EFE2124

4. Winding Specification

Pin No.	Wire	Turns	Inductance	Leakage Inductance	Remarks
5 → 2	1 UEW 0.45 ϕ	12	180μH	7.2μH	1KHz, 1V
7 → 9	1 UEW 0.04 ϕ	2430 (270 x 9)	7.2H	330mH	1KHz, 1V

5. BOM of the Application Circuit

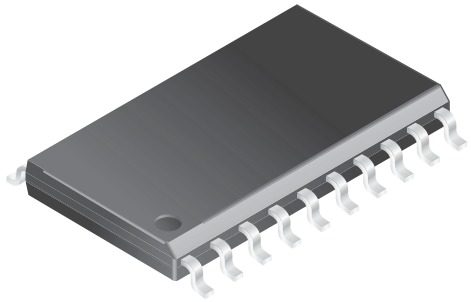
Part Ref.	Value	Description/Vendor	Part Ref.	Value	Description/Vendor
Fuse			C5	220p	50V 1608 J
F1	24V 3A	Fuse	C6	1μ	50V 2012 K
Resistor (SMD)			C7	10μ	16V 3216
R1	330K	1608 J	C8	10μ	16V 3216
R2	56K	1608 F	C9	1μ	16V 1608 K
R3	18K	1608 F	C10	15p	3KV 3216
R4	22K	1608 F	C11	15p	3KV 3216
R5	27K	1608 F	C12	15p	3KV 3216
R6	82K	1608 F	C13	15p	3KV 3216
R8	100K	1608 F	C14	10n	50V 1608 K
R9	9.1K	1608 F	C15	10n	50V 1608 K
R11	1K	1608 F	C17	2.2n	50V 1608 Z
R12	1K	1608 F	C18	2.2n	50V 1608 Z
R13	1K	1608 F	C19	2.2n	50V 1608 Z
R14	100K	1608 F	C20	2.2n	50V 1608 Z
R15	10K	1608 F	C21	10n	50V 1608 Z
R16	1K	1608 F	C25	1μ	50V 2012 K
R17	1K	1608 F	C26	0.1μ	16V 1608 K
R18	1K	1608 F	C27	1μ	50V 2012 K
R19	1K	1608 F	C28	10n	50V 1608 Z
R20	10K	1608 J	C29	10n	50V 1608 K
R21	10K	1608 J	C30	10n	50V 1608 K
R22	10K	1608 J	**Diode / TR (SMD)**		
R23	10K	1608 J	D1	BAW56	Fairchildsemi
R24	10K	1608 J	D3	BAV70	Fairchildsemi
R25	10K	1608 J	D4	BAV70	Fairchildsemi
R26	1K	1608 F	D6	BAV99	Fairchildsemi
R27	10K	1608 J	D7	BAV99	Fairchildsemi
Capacitor (SMD)			D8	BAV99	Fairchildsemi
C1	0.22μ	16V 1608 K	D9	BAV99	Fairchildsemi
C2	1μ	50V 2012 K	D10	BAW56	Fairchildsemi
C3	4.7n	50V 1608 K	D11	BAW56	Fairchildsemi
C4	4.7n	50V 1608 K	Q1	KST2222	Fairchildsemi

5. BOM of the Application Circuit (Continued)

Part Ref.	Value	Description/Vendor	Part Ref.	Value	Description/Vendor
Electrolytic capacitor			**Wafer (SMD)**		
C22	220µ	25V	CN1	35001WR-02A	
MOSFET (SMD)			CN2	35001WR-02A	
M1	FDS8958A	Fairchildsemi	CN3	35001WR-02A	
M2	FDS8958A	Fairchildsemi	CN4	35001WR-02A	
Transformer (SMD)			CN5	12505WR-10	
TX1	EFD2124	Supported by Namyang electronics (http://www.namyangelec.co.kr)			
TX2	EFD2124				

Mechanical Dimensions

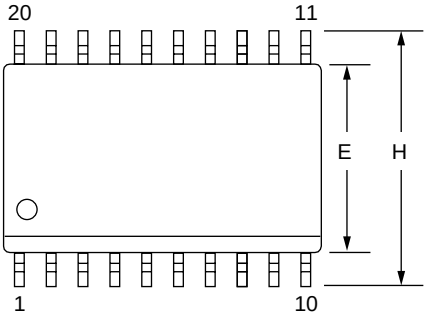
20-pin SOIC Package

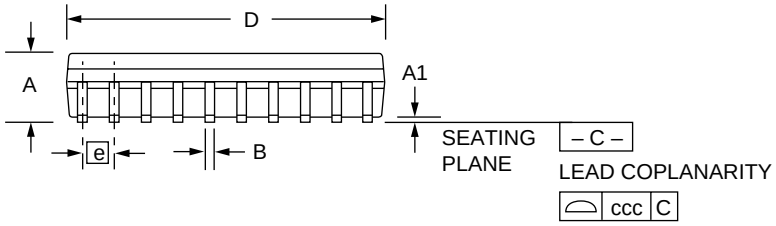


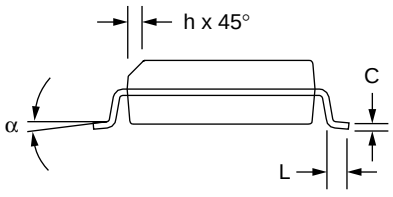
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







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EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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