DDR2 And DDR3 Power Solution Synchronous Buck Controller With 1.5A LDO

Features

Buck Controller (VDDQ)

- **High Input Voltages Range from 3V to 28V Input Power**
- **Provide 1.8V (DDR2), 1.5V (DDR3) or Adjustable Output Voltage from 0.75V to 5.5V**
  - **±1% Accuracy Over-Temperature**
- **Integrated MOSFET Drivers and Bootstrap Diode**
- **Excellent Line and Load Transient Responses**
- **PFM Mode for Increased Light Load Efficiency**
- **Constant-On-Time Controller Scheme**
  - **Switching Frequency Compensation for PWM Mode**
  - **Adjustable Switching Frequency from 100kHz to 550kHz in PWM Mode with DC Output Current**
- **Integrated MOSFET Drivers and Bootstrap Diode**
- **S3 and S5 Pins Control The Device in S0, S3, or S4/S5 State**
- **Power Good Monitoring**
- **70% Under-Voltage Protection (UVP)**
- **125% Over-Voltage Protection (OVP)**
- **Adjustable Current-Limit Protection**
  - **Using Sense Low-Side MOSFET $R_{DS(ON)}$**

±1.5A LDO Section (VTT)

- **Souring or Sinking Current up to 1.5A**
- **Fast Transient Response for Output Voltage**
- **Output Ceramic Capacitors Support at Least 10㎌ MLCC**
- **VTT and VTTREF Track at Half the VDDQSNS by Internal Divider**
- **±20mV Accuracy for VTT and VTTREF**
- **Independent Over-Current-Limit (OCL)**
- **Thermal Shutdown Protection**
- **QFN-24 4mmx4mm Thin Package (TQFN4x4-24A) for APW8813 and QFN-20 3mmx3mm Thin Package (TQFN3x3-20) for APW8813A**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APW8813/A integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It provides a complete power supply for DDR2 and DDR3 memory system. It offers the lowest total solution cost in system where space is at a premium.

The APW8813/A provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8813/A provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. On TQFN4x4-24A package, the Forced PWM Mode works nearly at constant frequency for low-noise requirements.

The APW8813/A is equipped with accurate current-limit, output under-voltage, and output over-voltage protections. A Power-On-Reset function monitors the voltage on V_{CC} prevents wrong operation during power on.

The LDO is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The device integrates two power transistors to source or sink current up to 1.5A. It also incorporates current-limit and thermal shutdown protection.

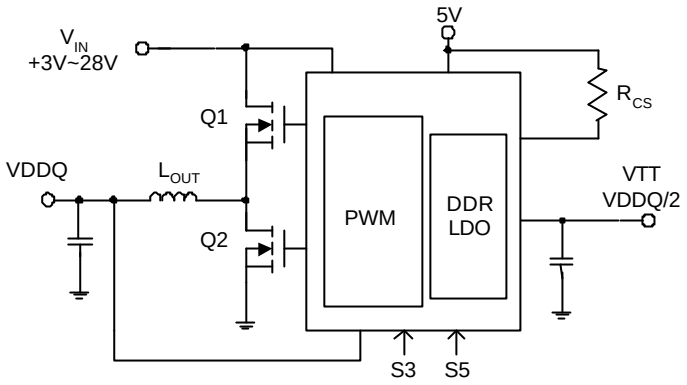
The output voltage of LDO tracks the voltage at VTTREF pin. An internal resistor divider is used to provide a half voltage of VDDQ for VTTREF and VTT Voltage. The VTT output voltage is only requiring 20µF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device, when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF.

The APW8813/A is available in 4mmx4mm 24-pin TQFN package, and the APW8813A is available in 3mmx3mm 20-pin TQFN package.

Applications

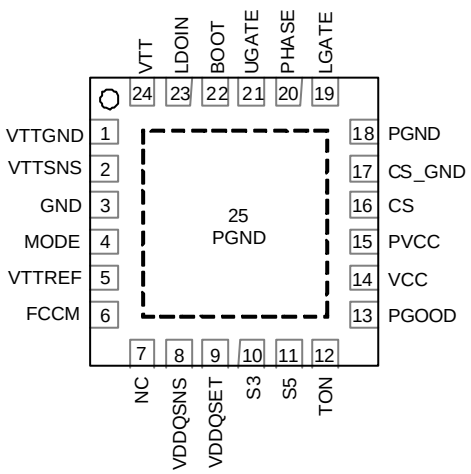
- **DDR2, and DDR3 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Termination**

Simplified Application Circuit



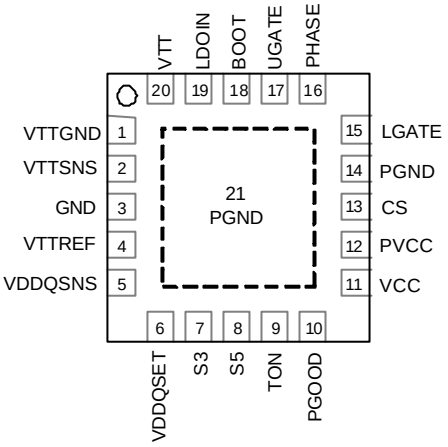
Pin Configuration

APW8813



TQFN4x4-24A
(Top View)

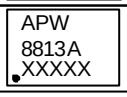
APW8813A



TQFN3x3-20
(Top View)

= Thermal Pad (connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW8813/A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-24A QB : TQFN3x3-20 Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8813 QB : 	XXXXX - Date Code
APW8813A QB : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{PVCC}	PVCC Supply Voltage (PVCC to GND)	-0.3 ~ 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
	UGATE Voltage (UGATE to PHASE) <400ns Pulse Width >400ns Pulse Width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <400ns Pulse Width >400ns Pulse Width	 -5 ~ PVCC+0.3 -0.3 ~ PVCC+0.3	V
	PHASE Voltage (PHASE to GND) <400ns Pulse Width >400ns Pulse Width	 -5 ~ 35 -0.3 ~ 28	V
	PGND, VTTGND and CS_GND to GND Voltage	-0.3 ~ 0.3	V
	All Other Pins (CS, MODE, S3, S5, VTTSNS, VDDQSNS, LDOIN, FCCM, VDDQSET, PGOOD, VTT, VTTREF GND)	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature,10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient TQFN4x4-24A TQFN3x3-20	 52 68	°C/W
θ_{JC}	Thermal Resistance - Junction to Case TQFN4x4-24A TQFN3x3-20	 7 8	°C/W

Note 3: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC}, V_{PVCC}	VCC and PVCC Supply Voltage	4.5 ~ 5.5	V
V_{IN}	Converter Input Voltage	3 ~ 28	V
V_{VDDQ}	Converter Output Voltage	0.75 ~5.5V/ DDR2 (1.8V)/ DDR3 (1.5V)	V
V_{VTT}	LDO Output Voltage	0.375 ~ 2.75	V
I_{OUT}	Converter Output Current	0 ~ 15	A
I_{VTT}	LDO Output Current	-1.5 ~ +1.5	A
C_{VCC}, C_{PVCC}	VCC and PVCC Capacitance	1~	µF
C_{VTT}	VTT Output Capacitance	10~100	µF
C_{VTTREF}	VTTREF Output Capacitance	0.01~0.1	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{PVCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8813/A			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
$I_{PVCCSDN}$	PVCC Shutdown Current	T_A =25°C, V_{S3} = V_{S5} = 0V, no load	-	0.1	1	µA
I_{VCC}	VCC Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load, PVCC Plus VCC Current, No Switching	-	0.8	3	mA
I_{VCCSTB}	VCC Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load, PVCC Plus VCC Current, No Switching	-	240	800	µA
I_{VCCSDN}	VCC Shutdown Current	T_A =25°C, V_{S3} = V_{S5} = 0V, no load	-	0.1	1	µA
I_{LDOIN}	LDOIN Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load	-	-	40	µA
$I_{LDOINSTB}$	LDOIN Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load	-	0.1	10	µA
$I_{LDOINSDN}$	LDOIN Shutdown Current	T_A = 25°C, V_{S3} = V_{S5} = 0V, no load	-	0.1	1	
POWER-ON-RESET						
	VCC POR Threshold	VCC Rising	4.0	4.2	4.4	V
	VCC POR Hysteresis		-	100	-	mV

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{PVCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW8813/A Min.	Typ.	Max.	Unit
VTT OUTPUT							
V_{VTT}	VTT Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V		-	0.9	-	V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V		-	0.75	-	
V_{VTT}	VTT Output Tolerance	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A		-20	-	20	mV
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1.5A		-30	-	30	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A		-20	-	20	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1.5A		-30	-	30	
I_{LIM}	Current-Limit	Sourcing Current (V_{IN} = 1.8V)	T_J = 25°C	1.8	2	3	A
			T_J = 125°C	1.6	-	-	
		Sinking Current (V_{IN} = 1.8V)	T_J = 25°C	-2	-2.2	-3	
			T_J = 125°C	-1.6	-	-	
		Sourcing Current (V_{IN} = 1.5V)	T_J = 25°C	1.6	1.8	2.6	A
			T_J = 125°C	1.1	-	-	
		Sinking Current (V_{IN} = 1.5V)	T_J = 25°C	-1.6	-1.8	-2.6	
			T_J = 125°C	-1.1	-	-	
$R_{DS(ON)}$	VTT Power MOSFETs $R_{DS(ON)}$	Upper MOSFET		-	350	500	mΩ
		Lower MOSFET		-	350	500	
I_{VTTLK}	VTT Leakage Current	V_{VTT} = 1.25V, V_{S3} = 0V, V_{S5} = 5V, T_A = 25°C		-1.0	-	1.0	µA
$I_{VTTSNSLK}$	VTTSNS Leakage Current	V_{VTT} = 1.25V, T_A = 25°C		-1.00	0.01	1.00	µA
I_{VTTDIS}	VTT Discharge Current	V_{VTT} = 0.5V, V_{S3} = V_{S5} = 0V, T_A = 25°C, V_{VREF} = 0V		15	25	35	mA
VTTREF OUTPUT							
V_{VTTREF}	VTTREF Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2		-	0.9	-	V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2		-	0.75	-	
	VTTREF Tolerance	0mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = V_{VTTREF} =1.8V		-18	-	+18	mV
		0mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V		-20	-	+20	
I_{VTTREF}	VTTREF Source Current	V_{VTTREF} = 0V		10	20	40	mA
	VTTREF Sink Current	V_{VTTREF} = 1.5V, V_{TT}=0.75V		-10	-20	-40	mA
VDDQ OUTPUT							
V_{VDDQ}	1.8V VDDQ Output Voltage	$V_{VDDQSET}$ = 5V, No load, T_A = 25°C		1.787	1.8	1.813	V
		$V_{VDDQSET}$ = 5V, No load, T_A = -40°C to 85°C		1.782	1.8	1.818	V
		$V_{VDDQSET}$ = 5V, Load = 0 to 10A, T_A = 25°C		1.764	1.8	1.836	V

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{PVCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8813/A			Unit
			Min.	Typ.	Max.	
VDDQ OUTPUT (CONT.)						
V_{VDDQ}	1.5V VDDQ Output Voltage	$V_{VDDQSET}$ = 0V, No load, T_A = 25°C	1.488	1.5	1.512	V
		$V_{VDDQSET}$ = 0V, No load, T_A = -40°C to 85°C	1.485	1.5	1.515	V
		$V_{VDDQSET}$ = 0V, Load = 0 to 10A, T_A = 25°C	1.47	1.5	1.53	V
$V_{VDDQSET}$	VDDQSET Regulation Voltage	Adjust Mode, T_A = 25°C	0.745	0.75	0.755	V
		Adjust Mode, T_A = -40°C to 85°C	0.7425	0.75	0.7575	V
		Adjust Mode, T_A = 25°C, V_{VCC} = 4.5V to 5.5V, V_{IN} = 3V to 28V	-0.1	-	+0.1	%
		Adjust Mode, T_A = 25°C, Load = 0 to 10A, V_{VCC} = 4.5V to 5.5V	-1	-	+1	%
$R_{VDDQSNS}$	VDDQSNS Input Impedance	$V_{VDDQSET}$ = 0V (DDR3)	-	240	-	kΩ
		$V_{VDDQSET}$ = 5V (DDR2)	-	288	-	
	VDDQSET Input Current	$V_{VDDQSET}$ = 0.78V	-0.1	-	+0.1	µA
	VDDQ Discharge Current	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, V_{MODE} = 0V (Non-Tracking)	15	25	-	mA
	LDOIN Discharge Current	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, V_{MODE} = 0.5V (Tracking, only for APW8813)	400	550	-	mA
PWM CONTROLLERS						
F_{SW}	Operating Frequency	Adjustable Frequency	100	-	550	kHz
T_{SS}	Internal Soft-Start Time	S5 is High to V_{VDDQ} Regulation	0.9	1.2	1.5	ms
T_O	On Time	V_{IN} = 19V, V_{VDDQ} = 1.5V, R_{TON} = 1.2M	235	277	320	ns
$T_{OFF(MIN)}$	Minimum off Time		-	300	-	ns
$T_{ON(MIN)}$	Minimum on Time		80	110	140	ns
	Zero-Crossing Threshold		-9.5	0.5	10.5	mV
VDDQ PROTECTIONS						
	CS Pin Sink Current	T_A = 25°C	9	10	11	µA
		Temperature Coefficient, On The Basis of 25°C	-	4500	-	ppm/°C
	OCP Comparator Offset	(V_{PVCC} - V_{CS}) - (V_{PHASE} - PGND), V_{PVCC} - V_{CS} = 60mV	-15	0	+15	mV
	VDDQ Current-Limit Setting Range	V_{PVCC}-V_{CS}	30	-	200	mV
	VDDQ OVP Trip Threshold	V_{VDDQ} Rising	120	125	130	%
	VDDQ OVP Debounce Delay	V_{FB} Rising, DV = 10mV	-	1.5	-	µs
	VDDQ UVP Trip Threshold	V_{VDDQ} Falling	60	70	80	%
	VDDQ UVP Trip Hysteresis		-	3	-	%
	VDDQ UVP Debounce		-	10	-	µs
	VDDQ UVP Enable Delay		-	2	-	ms

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{PVCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

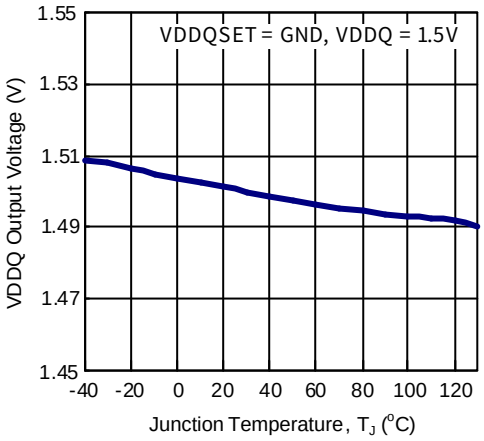
Symbol	Parameter	Test Conditions	APW8813/A			Unit
			Min.	Typ.	Max.	
PGOOD						
V_{PGOOD}	PGOOD Threshold	PGOOD in from Lower (PGOOD Goes High)	87	90	93	%
		PGOOD Low Hysteresis (PGOOD Goes Low)	-	3	-	%
		PGOOD in from Higher (PGOOD Goes Low)	120	125	130	%
		PGOOD High Hysteresis (PGOOD Goes High)	-	3	-	%
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V	-	0.1	1.0	µA
	PGOOD Sink Current	V_{PGOOD} = 0.5V	2.5	7.5	-	mA
	PGOOD Debounce Time		-	63	-	µs
GATE DRIVERS						
	UGATE Pull-Up Resistance	BOOT-UGATE = 0.5V	-	5	7	Ω
	UGATE Sink Resistance	UGATE-PHASE = 0.5V	-	1	2.5	Ω
	LGATE Pull-Up Resistance	PVCC-LGATE = 0.5V	-	5	7	Ω
	LGATE Sink Resistance	LGATE-PGND = 0.5V	-	1	2.5	Ω
	UGATE to LGATE Dead Time	UGATE falling to LGATE rising, no load	-	40	-	ns
	LGATE to UGATE Dead Time	LGATE falling to UGATE rising, no load	-	40	-	ns
BOOTSTRAP DIODE						
	Forward Voltage	V_{PVCC} - V_{BOOT}, I_F = 10mA, T_A = 25°C	-	0.5	0.8	V
	Reverse Leakage	V_{BOOT} = 30V, V_{PHASE} = 25V, V_{PVCC} = 5V, T_A = 25°C	-	-	0.5	µA
LOGIC THRESHOLD						
V_{IH}	S3, S5 High Threshold Voltage	S3, S5 Rising	1.6	-	-	V
V_{IL}	S3, S5 Low Threshold Voltage	S3, S5 Falling	-	-	0.3	V
	S5 to S3 Debounce Time	S5 from L to H, VDDQ, VREF are on	-	90	-	µs
	S3 to S0 Debounce Time	S3 from L to H, VTT is on	-	10	-	µs
I_{ILEAK}	Logic Input Leakage Current	V_{S3} = V_{S5} = V_{MODE} = 5V, T_A = 25°C	-1	-	4.7	µA
$V_{FCCMTHR}$	FCCM High Threshold (Only for APW8813)	In Automatic PFM/PWM Mode	4.7	-	-	V
$V_{FCCMTHF}$	FCCM Low Threshold (Only for APW8813)	In Force PWM Mode	-	-	0.1	V
V_{THMODE}	MODE Threshold (Only for APW8813)	No Discharge	4.7	-	-	V
		Non-tracking Discharge	-	-	0.1	
	VDDQSET Threshold	V_{VDDQ} = 1.5V	0.08	0.15	0.4	V
		V_{VDDQ} = 1.8V	3.5	4	4.5	
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	160	-	°C
	Thermal Shutdown Hysteresis		-	25	-	°C

Pin Description

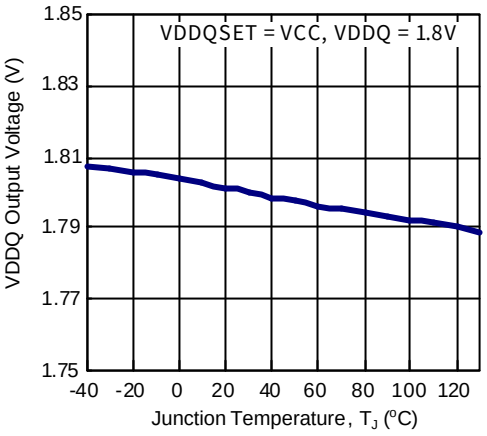
PIN			FUNCTION
APW8813	APW8813A	NAME	
1	1	VTTGND	Power ground output for the VTT LDO.
2	2	VTTSNS	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.
3	3	GND	Signal ground for the PWM controller and VTT LDO. Connect to minus terminal of the VTT LDO output capacitor.
4	-	MODE	Discharge mode setting pin. When this pin connects to VCC, it is no discharge state. When this pin connects to VDDQ, it is tracking discharge state. When this pin connects to GND, it is non-tracking discharge state.
5	4	VTTREF	VTTREF buffered reference output.
6	-	FCCM	Selection pin for PWM controller to operate in either forced PWM or automatic PWM/PFM mode. Force PWM mode is enable when FCCM pin is pulled below the falling threshold voltage $V_{FCCMTHF}$, and force PWM is disabled when the FCCM pin is pulled above the rising threshold voltage $V_{FCCMTHR}$.
7	-	NC	No Connection.
8	5	VDDQSNS	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ non-tracking discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to VCC or GND.
9	6	VDDQSET	VDDQ output voltage setting pin.
10	7	S3	S3 signal input.
11	8	S5	S5 signal input.
12	9	TON	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{TON} from TON pin to PHASE VIN terminal.
13	10	PGOOD	Power-good output pin. PGOOD is an open drain output used to Indicate the status of the output voltage. When VDDQ output voltage is within the target range, it is in high state.
14	11	VCC	Filtered 5V power supply input for internal control circuitry. Connect R-C network from PVCC to VCC.
15	12	PVCC	5V power supply voltage input pin for low-side MOSFET gate driver on TQFN-24 package.
16	13	CS	Over-current trip voltage setting input for $R_{DS(ON)}$ current sense scheme if connected to VCC through the voltage setting resistor.
17	-	CS_GND	Current sense comparator positive input terminal and the ground for power good circuit.
18	14	PGND	Power ground of the LGATE low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET. Also it is current sense comparator positive input terminal and the ground of power good circuit on SSOP-20 package.
19	15	LGATE	Output of the low-side MOSFET driver for PWM. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to VCC.
20	16	PHASE	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UGATE high-side gate driver.
21	17	UGATE	Output of the high-side MOSFET driver for PWM. Connect this pin to Gate of the high-side MOSFET.
22	18	BOOT	Supply Input for the UGATE Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
23	19	LDOIN	Supply voltage input for the VTT LDO.
24	20	VTT	Power output for the VTT LDO.

Typical Operating Characteristics

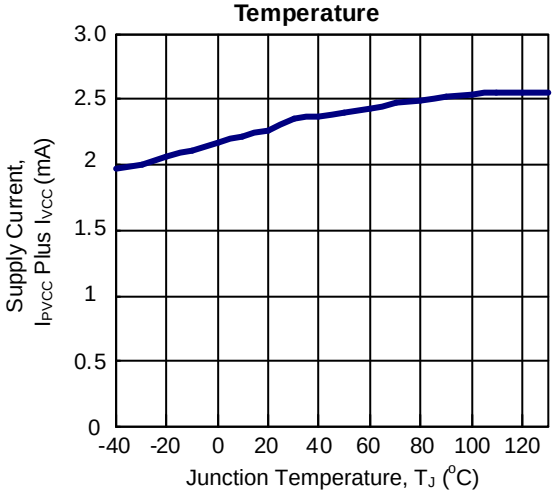
VDDQ Voltage Regulation vs. Junction Temperature



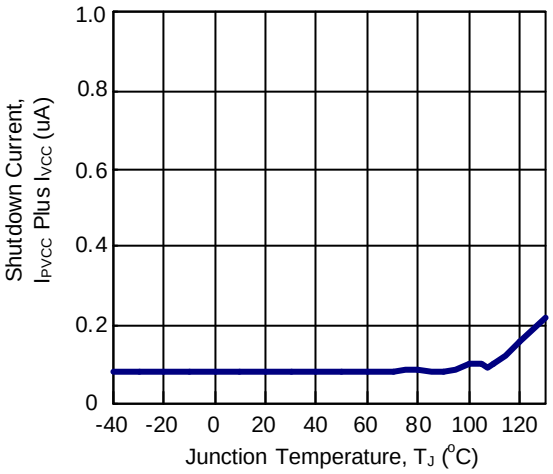
VDDQ Voltage Regulation vs. Junction Temperature



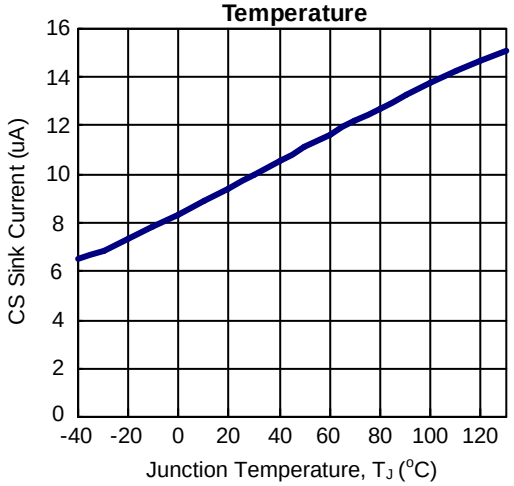
Supply Current vs. Junction Temperature



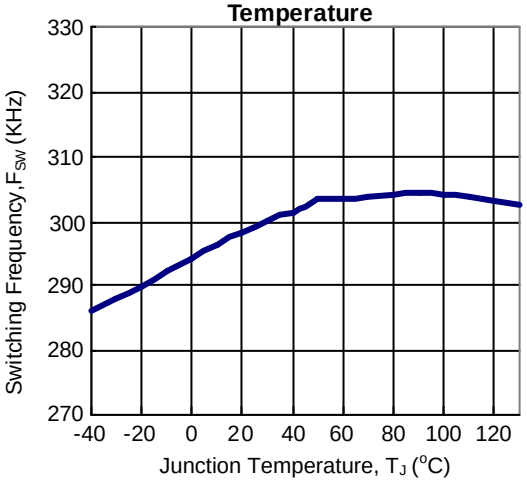
Shutdown Current vs. Junction Temperature



CS Pin Sink Current vs. Junction Temperature

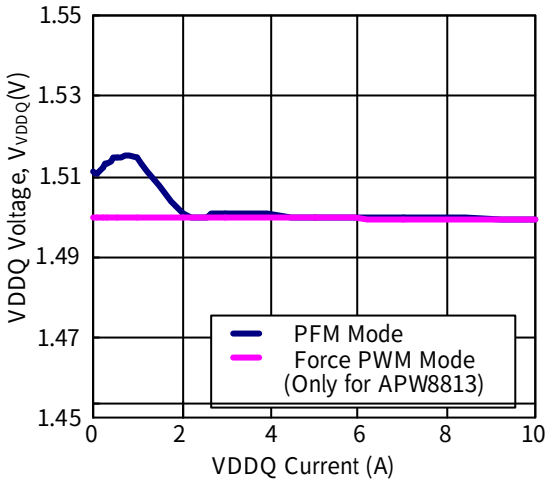


Frequency vs. Junction Temperature

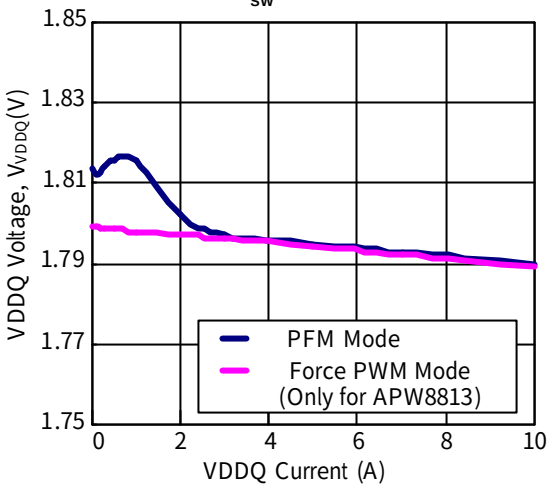


Typical Operating Characteristics

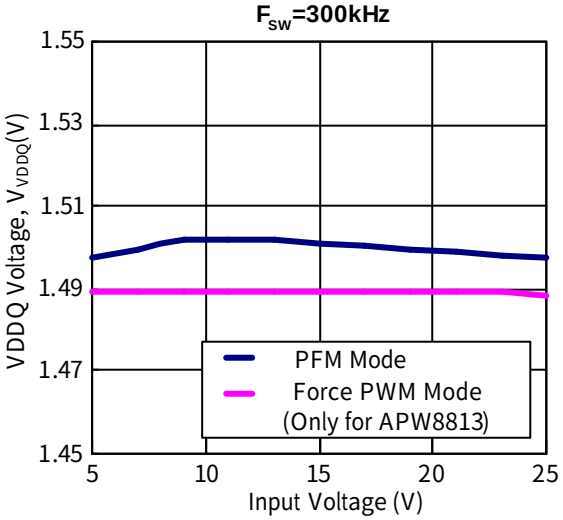
Load Regulation, V_{VDDQ}=1.5V
F_{SW}=300kHz



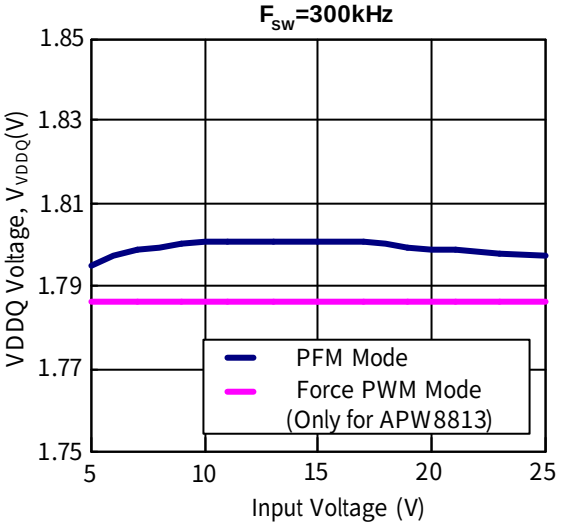
Load Regulation, V_{VDDQ}=1.8V
F_{SW}=300kHz



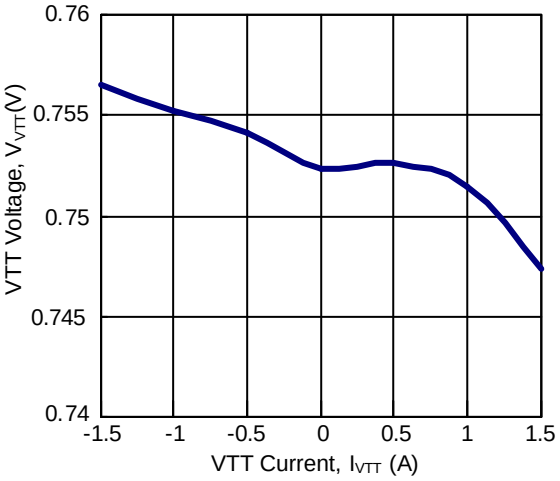
Line Regulation, V_{VDDQ}=1.5V
F_{SW}=300kHz



Line Regulation, V_{VDDQ}=1.8V
F_{SW}=300kHz

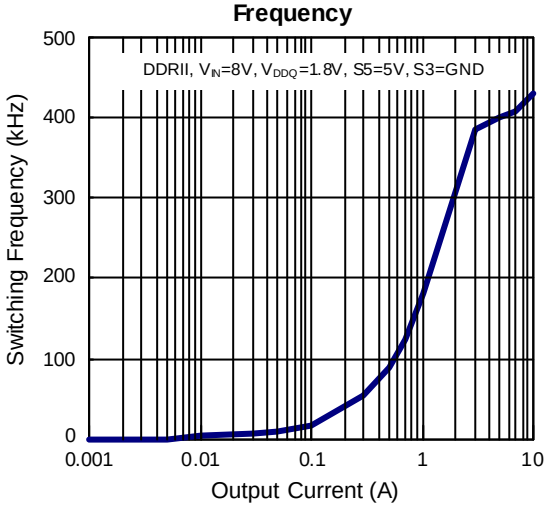


VTT Load Regulation

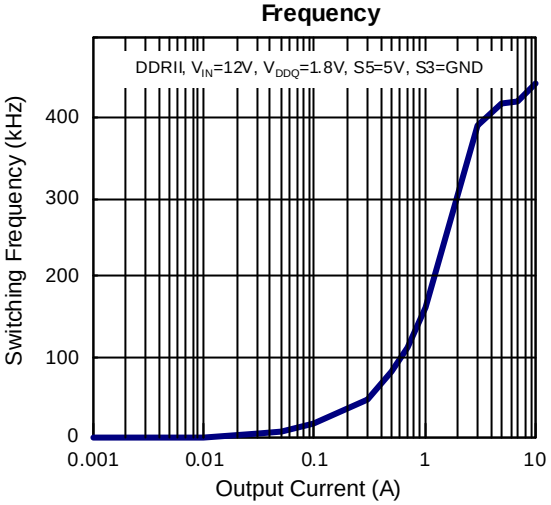


Typical Operating Characteristics

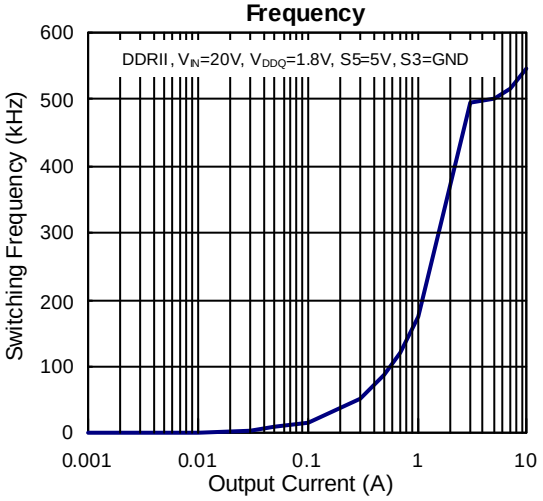
Output Current vs. Switching Frequency



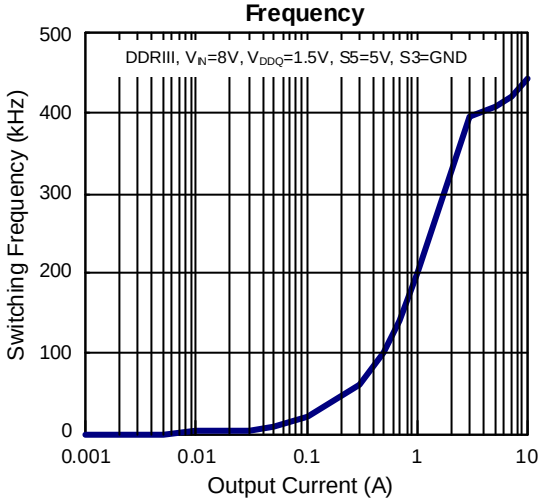
Output Current vs. Switching Frequency



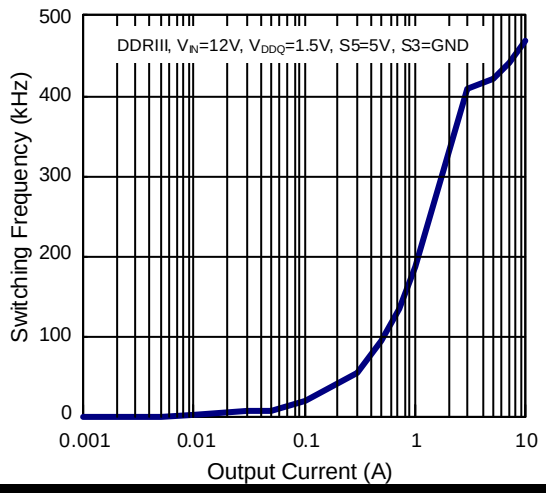
Output Current vs. Switching Frequency



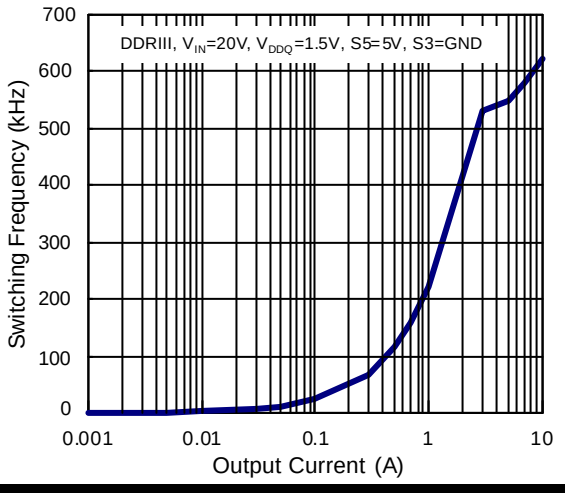
Output Current vs. Switching Frequency



Output Current vs. Switching Frequency

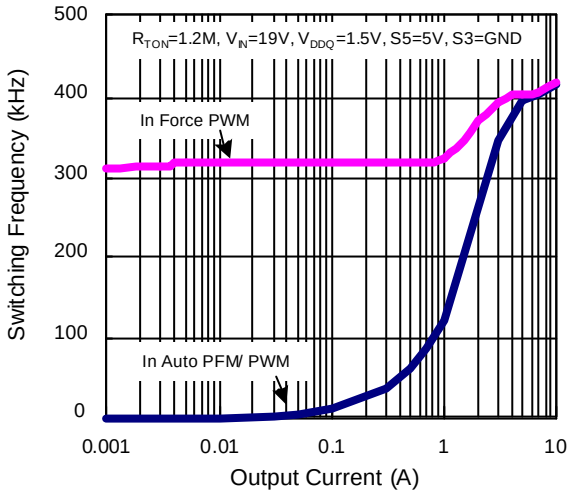


Output Current vs. Switching Frequency

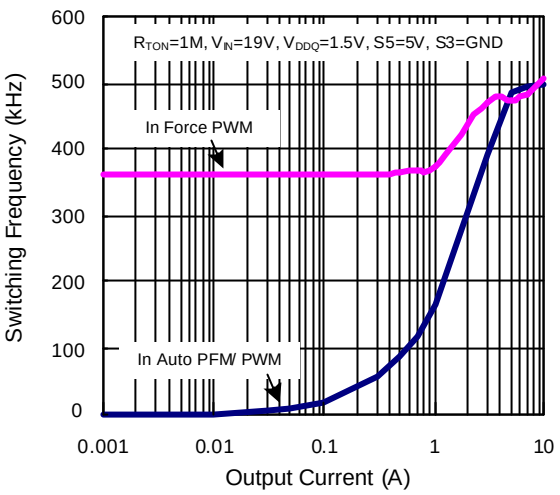


Typical Operating Characteristics

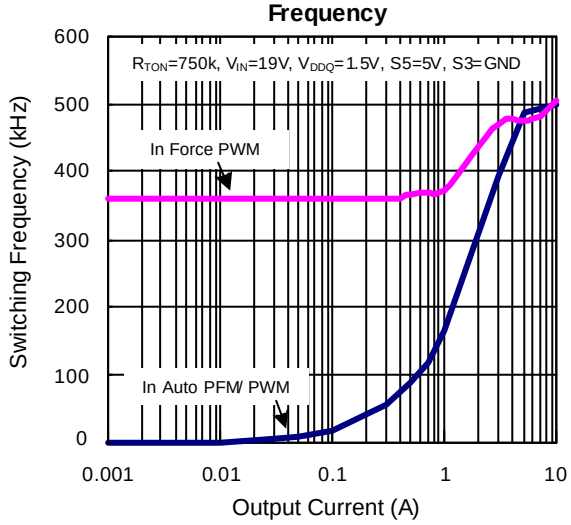
Output Current vs. Switching Frequency



Output Current vs. Switching Frequency

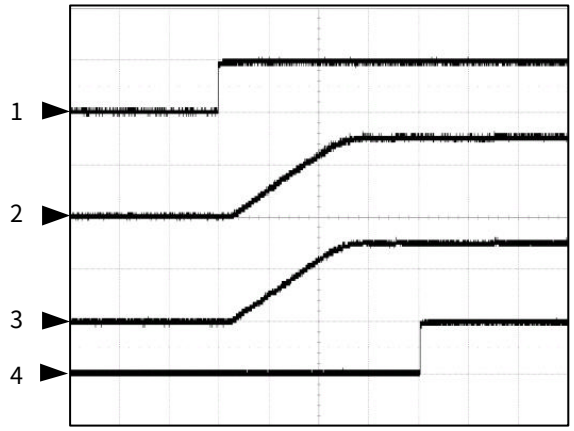


Output Current vs. Switching Frequency



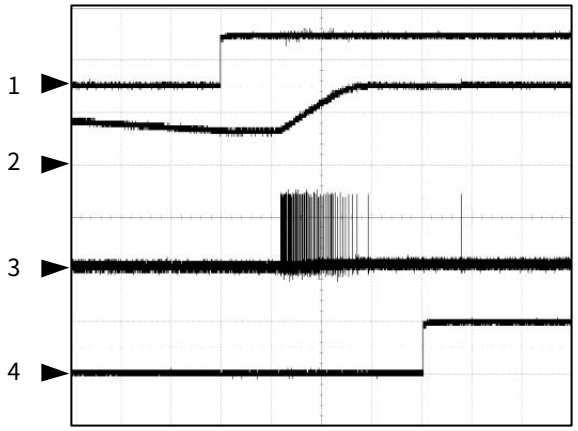
Operating Waveforms

S5 Enable, No Load



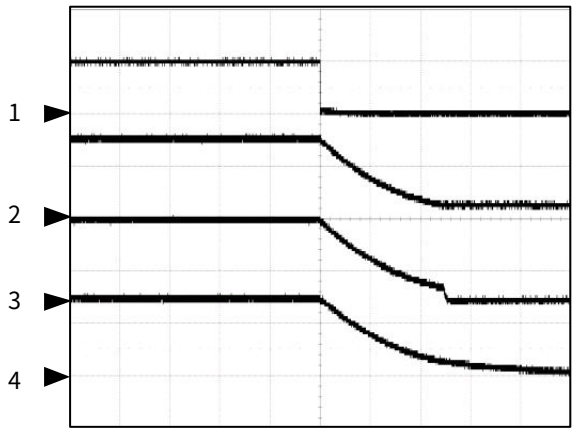
CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTTREF} (500mV/div)
CH4: V_{POK} (5V/div)
Time: 500µs/div

Non-Zero VDDQ S5 Enable



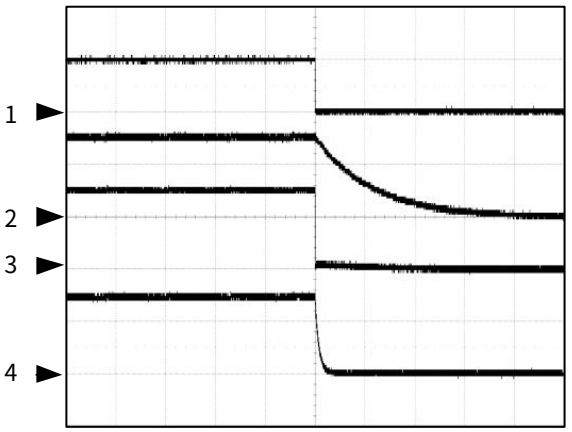
CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{UGATE} (20V/div)
CH4: V_{POK} (5V/div)
Time: 500µs/div

S5 Shutdown- Tracking Discharge
(Only for APW8813)



CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTTREF} (500mV/div)
CH4: V_{VTT} (500mV/div)
Time: 200µs/div

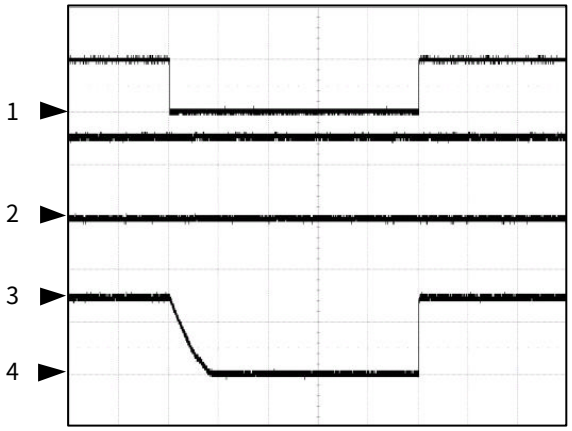
S5 Shutdown- Non-Tracking Discharge



CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTTREF} (500mV/div)
CH4: V_{VTT} (500mV/div)
Time: 5ms/div

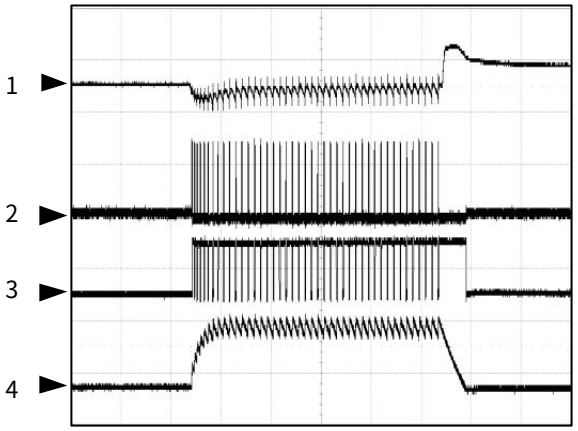
Operating Waveforms

S3 Enable-Shutdown



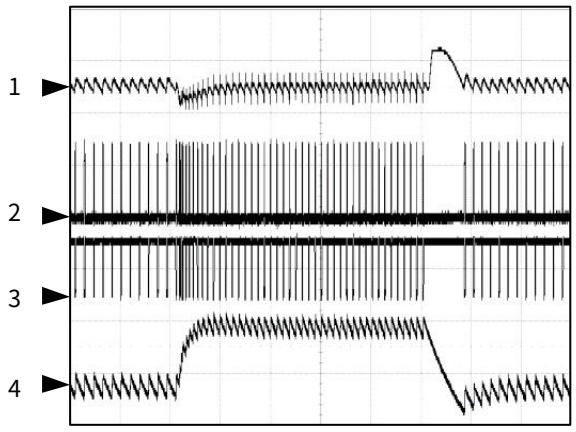
CH1: V_{S3} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTTREF} (500mV/div)
CH4: V_{VTT} (500mV/div)
Time: 10ms/div

Load Transient, I_{VDDQ} = 0A->10A->0A PFM Mode



CH1: V_{VDDQ} (200mV/div)
CH2: V_{UGATE} (20V/div)
CH3: V_{LGATE} (5V/div)
CH4: I_L (10A/div)
Time: 20µs/div

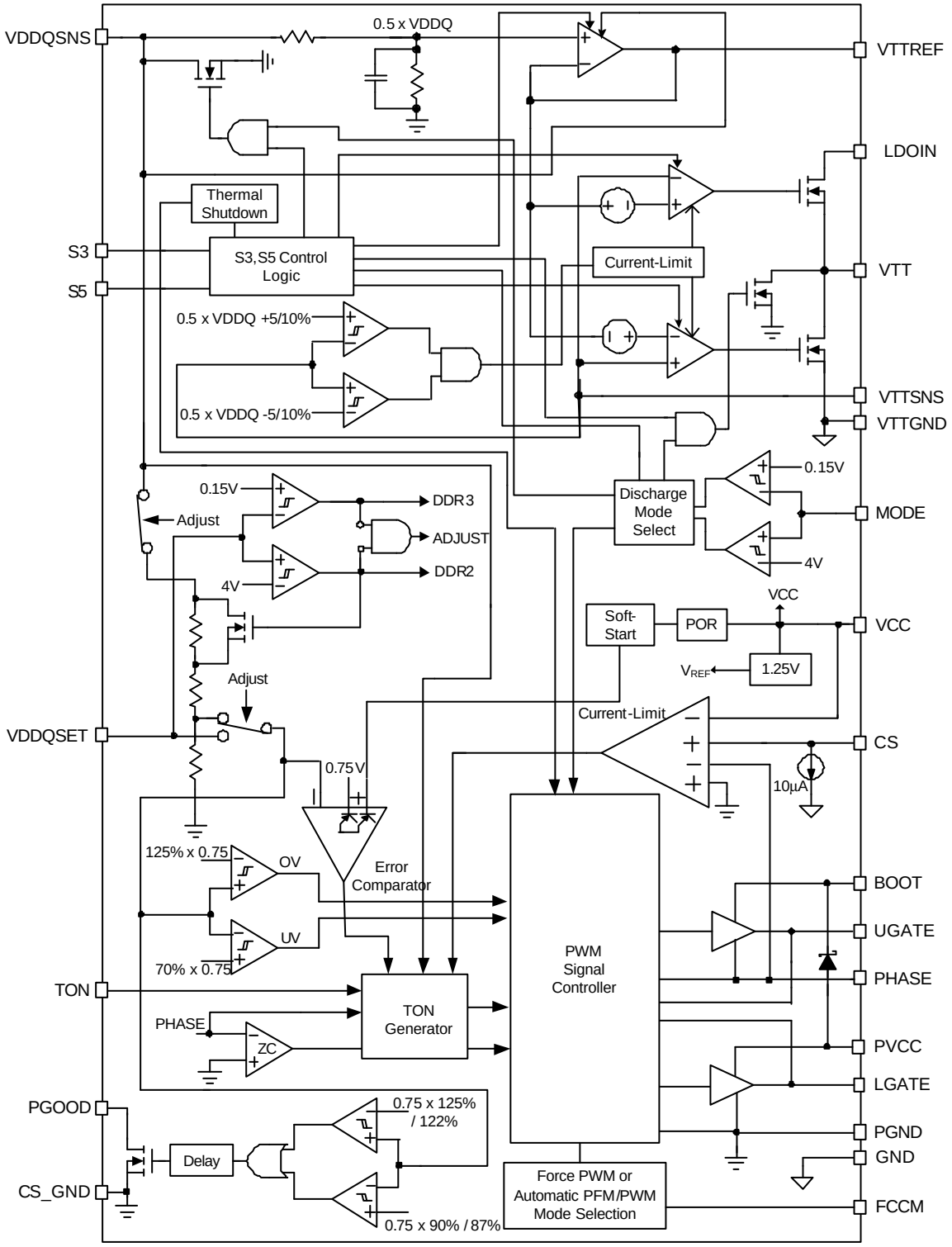
Load Transient, I_{VDDQ} = 0A->10A->0A Force PWM Mode (Only for APW8813)



CH1: V_{VDDQ} (200mV/div)
CH2: V_{UGATE} (20V/div)
CH3: V_{LGATE} (5V/div)
CH4: I_L (10A/div)
Time: 20µs/div

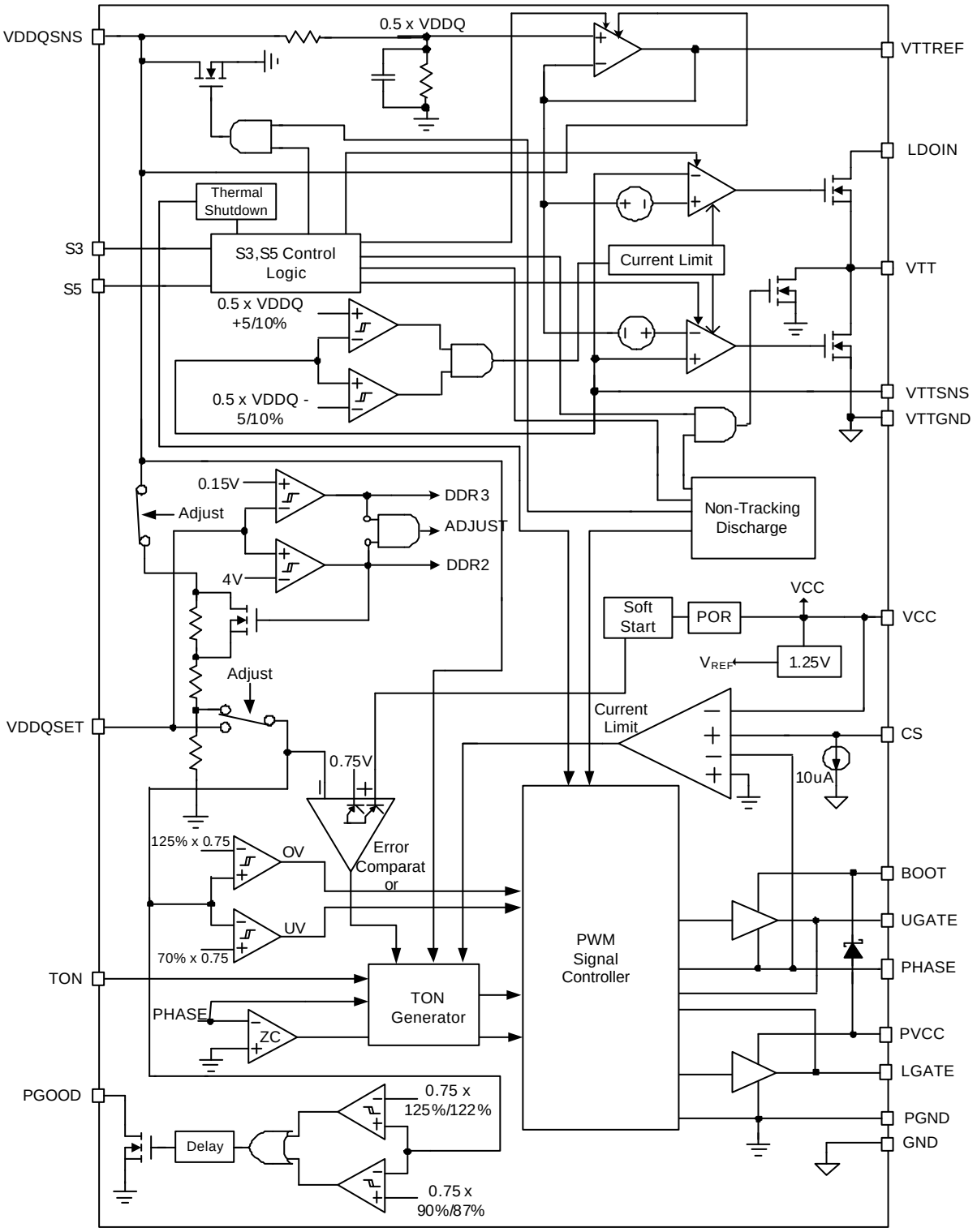
Block Diagram

APW8813



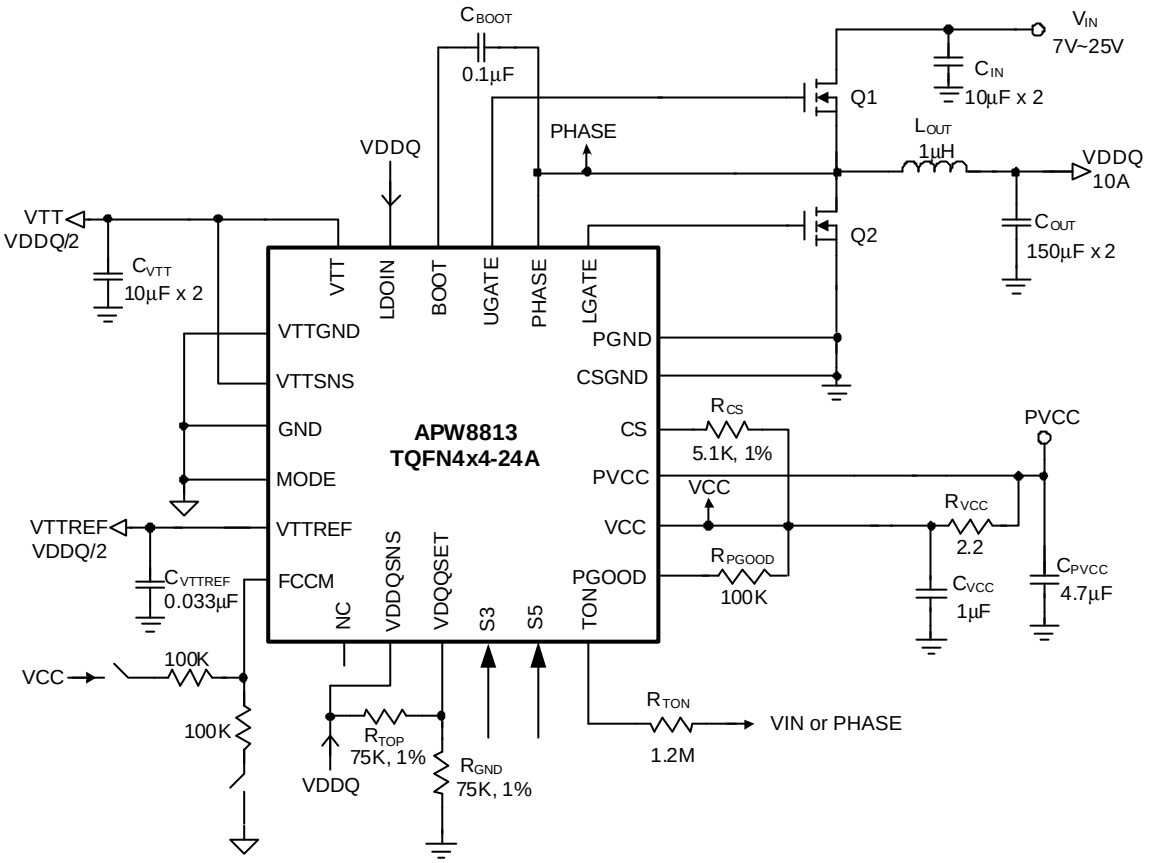
Block Diagram (Cont.)

APW8813A



Typical Application Circuit

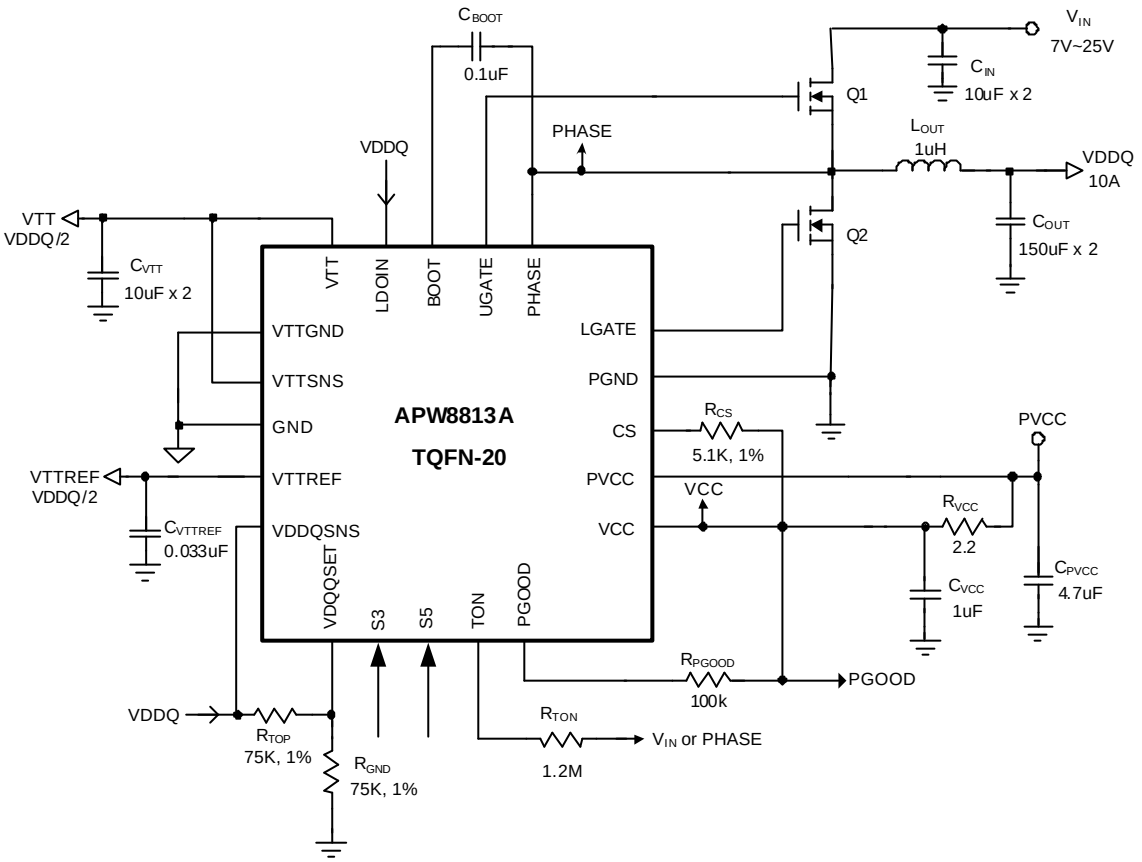
APW8813



VDDQ=Adjustable, External LDOIN, Non-tracking Discharge

Typical Application Circuit

APW8813A



VDDQ=Adjustable, External LDOIN

Function Description

The APW8813/A integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It provides a complete power supply for DDR2 and DDR3 memory system in both TQFN packages. The preset output voltage is selectable from 1.8V or 1.5V. User defined output voltage is also possible and can be adjustable from 0.75V to 5.5V. Input voltage range of the PWM converter is 3V to 28V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA. The VTT LDO can source and sink up to 1.5A peak current with only 10µF ceramic output capacitor. VTTREF tracks VDDQ/2 within 1% of VDDQ. VTT output tracks VTTREF within 20 mV at no load condition while 40 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using LDOIN pin. This helps reducing power dissipation in sourcing phase. The APW8813/A is fully compatible to JEDEC DDR2/DDR3 specifications at S3/S5 sleep state (see Table 1). Only for APW8813, when both VTT and VDDQ are disabled, the part has two options of output discharge function. The tracking discharge mode discharges VDDQ and VTT outputs through the internal LDO transistors and then VTT output tracks half of VDDQ voltage during discharge. The non-tracking discharge mode discharges outputs using internal discharge MOSFETs that are connected to VDDQSNS and VTT. The current capability of these discharge MOSFETs are limited and discharge occurs more slowly than the tracking discharge. Selecting non-discharge mode can disable these discharge functions.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor' s effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant-on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.
Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.2V typical), the POR signal goes high and the chip initiates soft-start operations. When this voltage drops lower than 4.1V (typical), the POR disables the chip.

Soft-Start

The APW8813/A integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows VDDQ soft-start sequence. When the S5 pin is pulled above the rising S5 threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1.2ms (typical) and independent of the UGATE switching frequency.

Function Description (Cont.)

Soft-Start (Cont.)

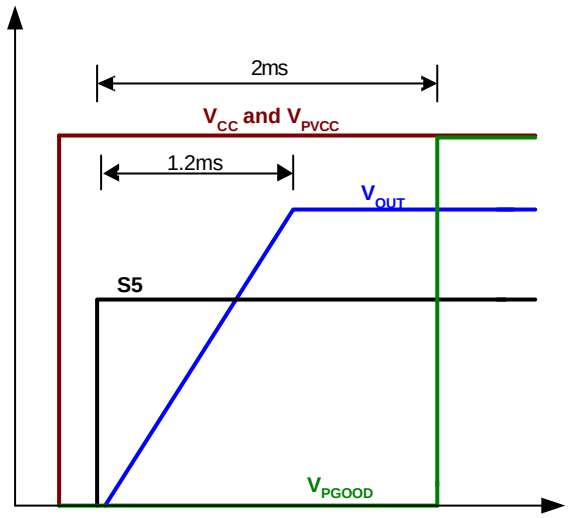


Figure 1. Soft-Start Sequence

During soft-start stage before the PGOOD pin is ready, the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage equals to the $V_{VDDQSET}$ or internal feedback voltage. This will ensure the output voltage starts from its existing voltage level.

The VTT LDO part monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VTT to GND or LDOIN) conditions.

The VTT LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current-limit start-up, the VTT cannot start successfully.

APW8813/A has an independent counter for each output, but the PGOOD signal indicates only the status of VDDQ and does not indicate VTT power good externally.

Power-Good Output (PGOOD)

PGOOD is an open-drain output and the PGOOD comparator continuously monitors the output voltage. PGOOD is actively held low in shutdown, and standby. When PWM converter' s output voltage is greater than 90% of its target value, the internal open-drain device will be pulled low. After 63µs debounce time, the PGOOD goes high. The PGOOD goes low if V_{VDDQ} output is 13% below or 25% above its nominal regulation point.

Under-Voltage Protection (UVP)

If VDDQSET is connected to VCC or GND, an internal resistor divider inside VDDQSNS pin makes the feedback voltage. If an external resistor divider is connected to VDDQSET pin, the feedback voltage is VDDQSET voltage itself.

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after 2ms of PWM operations to ensure start-up. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold (70% of normal output voltage), after 10 µs debounce time, APW8813/A shuts down the output gradually and latches off both high and low side MOSFETs.

Over-Voltage Protection

The feedback voltage should increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over-voltage protection comparator designed with a 1.5µs noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse.

When the OVP occurs, the PGOOD pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It' s a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, toggling VCC power-on-reset signal can only reset it.

Function Description (Cont.)

PWM Converter Current-Limit

The current-limit circuit employs an unique "valley" current sensing algorithm (Figure 2). CS pin should be connected to VCC through the trip voltage-setting resistor, R_{CS}. CS terminal sinks 10µA current, I_{CS}, and the current-limit threshold is set to the voltage across the R_{CS}. The voltage between PGND and PHASE pin monitors the inductor current so that PHASE pin should be connected to the drain terminal of the low side MOSFET. PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low side MOSFET.

If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the function of the sense resistance, inductor value, and input voltage. The equation for the current-limit threshold is as below:

$$I_{LIMIT} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{R_{CS} \times 10\mu A}{R_{DS(ON)}} + \frac{(V_{IN} - V_{VDDQ})}{2 \times L \times F_{SW}} \times \frac{V_{VDDQ}}{V_{IN}}$$

Where

I_{LIMIT} is the desired current-limit threshold

R_{CS} is the value of the current sense resistor connected to CS and VCC pins

V_{CS} is the voltage across the R_{CS} resistor

I_{RIPPLE} is inductor peak to peak current

F_{SW} is the PWM switching frequency

In a current-limit condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. If the output voltage becomes less than power good level, the V_{CS} is cut into half and the output voltage tends to be even lower. Eventually, it crosses the under-voltage protection threshold and shutdown.

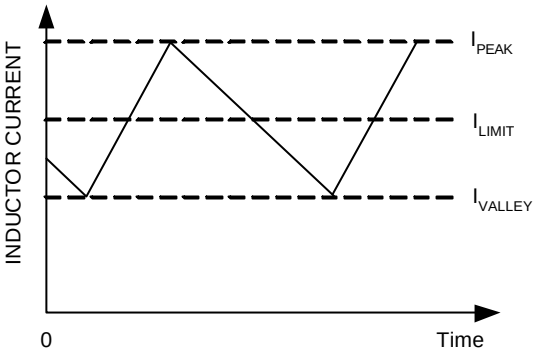


Figure 2. Current-Limit Algorithm

VTT Sink/Source Regulator

The output voltage at VTT pin tracks the reference voltage applied at VTTREF pin. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from LDOIN pin or sinking current to GND pin. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. The VTT with fast response feedback loop keeps tracking to the VTTREF within ±40mV at all conditions including fast load transient.

S3, S5 Control

In the DDR2/DDR3 memory applications, it is important to keep VDDQ always higher than VTT/VTTREF including both start-up and shutdown.

The S3 and S5 signals control the VDDQ, VTT, VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VDDQ, VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VDDQ and VTTREF are kept on while the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VDDQ, VTT and VTTREF are turned off and discharged to the ground according to the discharge mode selected by MODE pin during S4/S5 state, only for APW8813. On APW8813A, the default discharge mode is non-tracking discharge.

Function Description (Cont.)

S3, S5 Control (Cont.)

Table1: The Truth Table of S3 and S5 Pins.

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

VDDQ and VTT Discharge Control

APW8813/A discharges VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. The APW8813A default discharge mode is non-tacking discharge and there are two different discharge modes for APW8813. Connecting MODE pin as shown in Table 2 can set the discharge mode.

Table 2. Discharge Selection. (Only for APW8813)

MODE	DISCHARGE MODE
VCC	No Discharge
VDDQ	Tracking Discharge
GND	Non-Tracing Discharge

When in tracking-discharge mode, the device discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via LDOIN to VTTGND thus LDOIN must be connected to VDDQ output in this mode. The internal LDO can handle up to 1.5A and discharge quickly. After VDDQ is discharged down to 0.2V, the internal LDO is turned off and the operation mode is changed to the non-tracking discharge mode.

When in non-tracking-discharge mode, the device discharges outputs using internal MOSFETs that are connected to VDDQSNS and VTT. The current capability of these MOSFETs is limited to discharge slowly.

Note that VDDQ discharge current flows from VDDQSNS to PGND in this mode. In case of no discharge mode, APW8813/A does not discharge output charge at all.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW8813/A. When the junction temperature exceeds +160°C, PWM converter, VTTLDO and VTTREF are shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 25°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Programming the On-Time Control and PWM Switching Frequency

The APW8813/A does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage V_{VDDQ} and inverses proportional to input voltage V_{IN}. In PWM, the on-time calculation is written as below :

$$T_{ON} = 11.5\times10^{-12}\times R_{TON}\left[\frac{\left(\frac{1}{4}\right)V_{VDDQ}+75mV}{V_{IN}}\right]-50ns$$

Where:

R_{TON} is the resistor connected from TON pin to VIN or PHASE pin. Furthermore, the approximate PWM switching frequency is written as :

$$T_{ON}=\frac{D}{F_{SW}}\Rightarrow F_{SW}=\frac{V_{VDDQ}/V_{IN}}{T_{ON}}$$

Where:

F_{SW} is the PWM switching frequency.

APW8813/A doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring V_{PHASE} voltage as input voltage to calculate on-time when the high-side MOSFET is turned on. And then, use the relationship between ontime and duty cycle to obtain the switching frequency.

Application Information

Output Voltage Selection

Connect VDDQSET to GND to set the DDR3 fixed 1.5V or connect VDDQSET to VCC to set the DDR2 fixed 1.8V output voltage. The output voltage, $V_{OUT} = V_{VDDQ}$, of PWM can be also adjusted from 0.75V to 5.5V with a resistor-driver at VDDQSET between VDDQSNS and GND. Using 1% or better resistors for the resistive divider is recommended. The VDDQSET pin is the inverter input of the error amplifier, and the reference voltage is 0.75V. Take the example, the output voltage of PWM1 is determined by:

$$V_{OUTI} = 0.75 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where R_{TOP} is the resistor connected from V_{OUTI} to $V_{VDDQSET}$ and R_{GND} is the resistor connected from VDDQSET to GND.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor' s ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are remmended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

- For the low-side MOSFET, before it is turned on, the body diode has been conducted. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, the $R_{DS(ON)}$ of the low-side MOSFET, the less the power loss. The gate charge for this MOSFET is usually a secondary consideration. The high-side MOSFET does not have this zero voltage switching condition, and because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations :

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET..

Layout Consideration

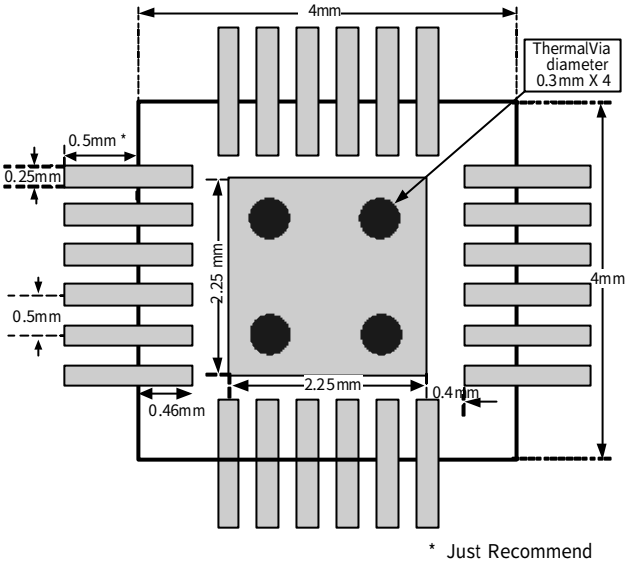
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

Application Information (Cont.)

Layout Consideration (Cont.)

- Keep the switching nodes (UGATE, LGATE, BOOT, and PHASE) away from sensitive small signal nodes (VDDQSET, VTTREF, CS, and MODE) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt, with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current limit stetting resistors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the VTTREF decoupling capasitor should be close to the VTTREF pin and GND; the VDDQ and VTT output capacitors should be located right across their output pin as clase as possible to the part to minimize parasitics. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking. And PHASE pin traces are also the return path for UGATE. Connect this pin to the converter's upper MOSFET source.
- The APW8813/A used ripple mode control. Build the resistor divider close to the VDDQSET pin so that the high imped ance trace is shorter when the output voltage is in ad justable mode. And the VDDQSET pin traces can't be closed to the switching signal traces (UGATE, LGATE, BOOT, and PHASE).
- The PGND trace should be a separate trace, and inde pendently go to the source of the low-side MOSFETs for current limit accuracy.

TQFN4x4-24A



TQFN3x3-20

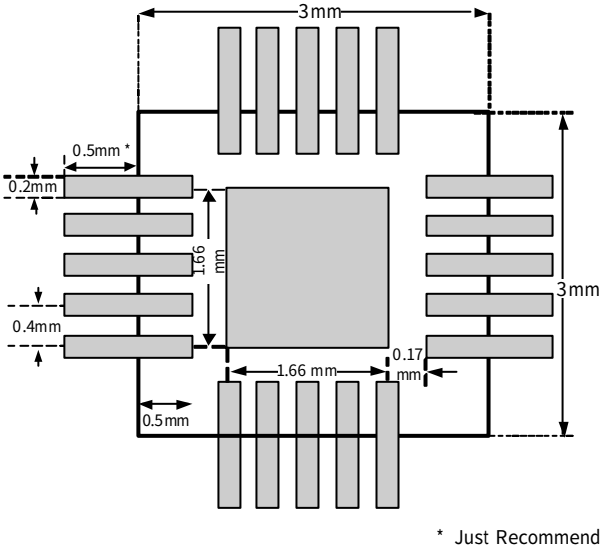
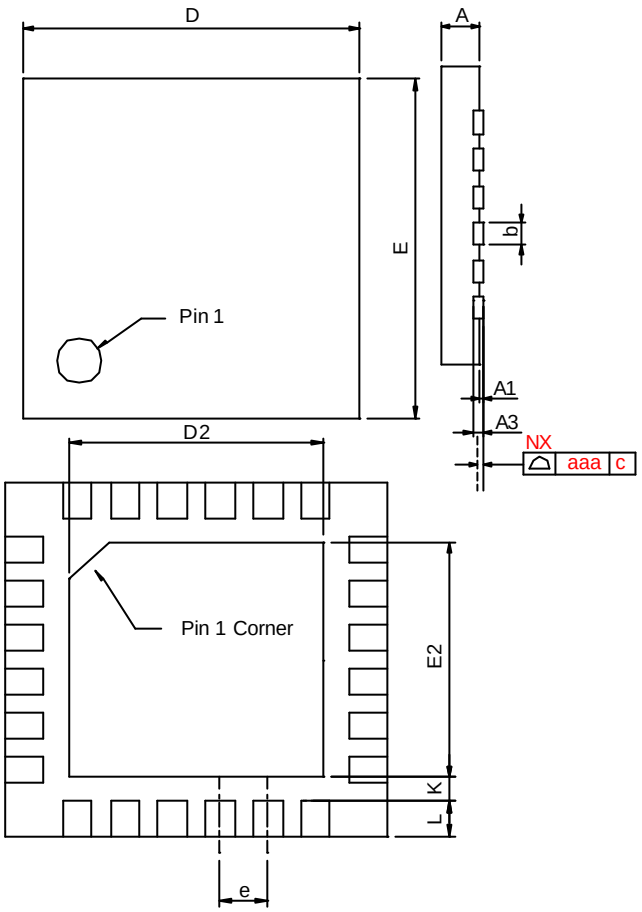


Figure 3. Recommened Minimum Footprint

Package Information

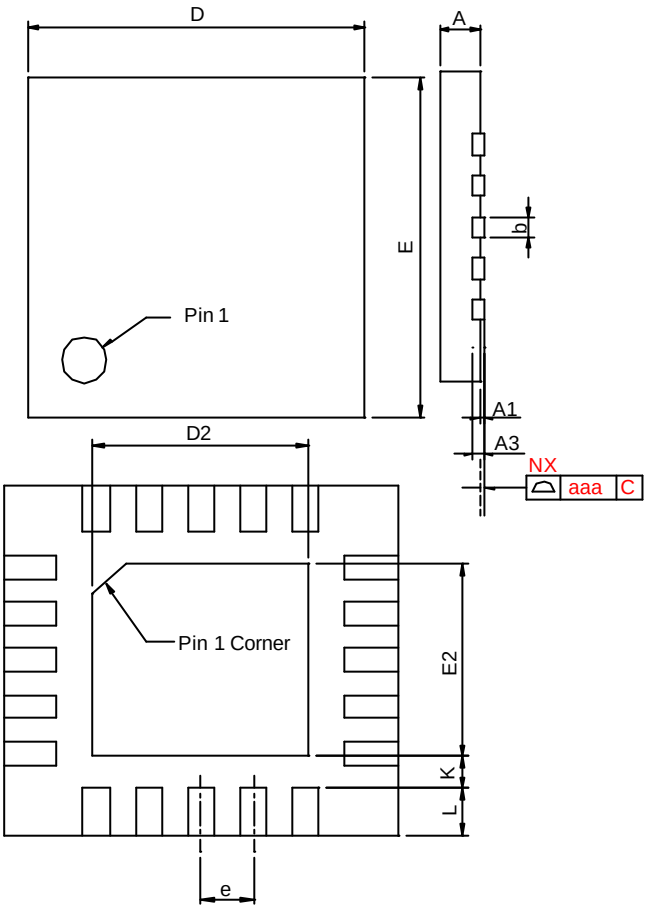
TQFN4x4-24A



SYMBOL	TQFN4x4-24A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.50	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.50	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Package Information

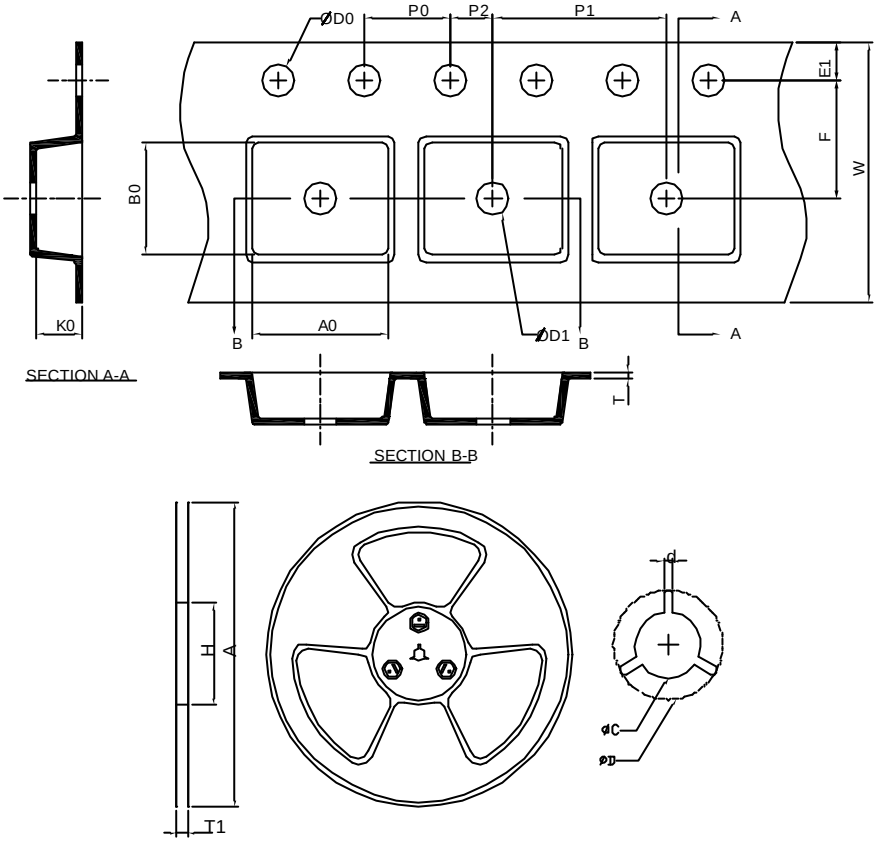
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-24A	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.25±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

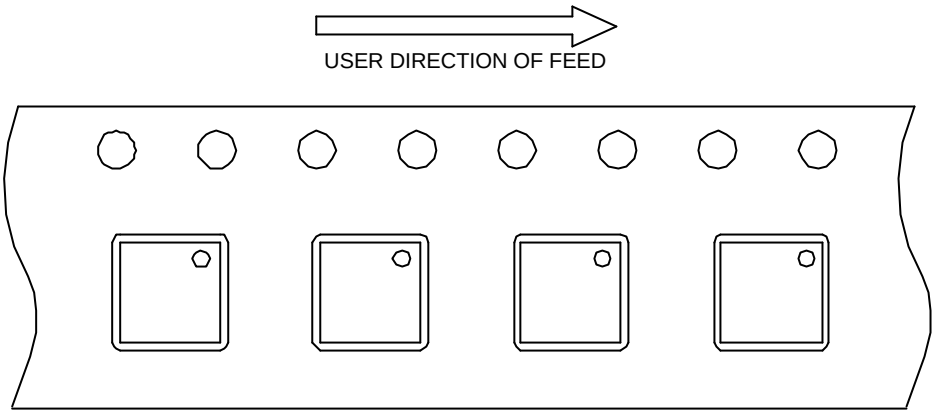
(mm)

Devices Per Unit

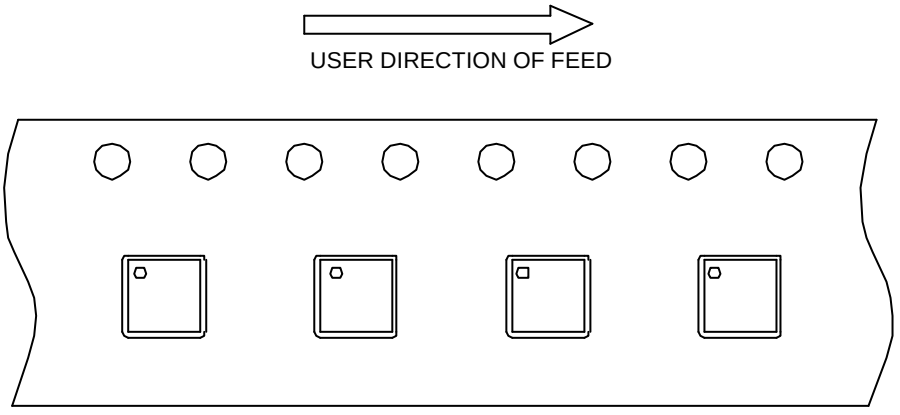
Package Type	Unit	Quantity
TQFN4x4-24A	Tape & Reel	3000
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

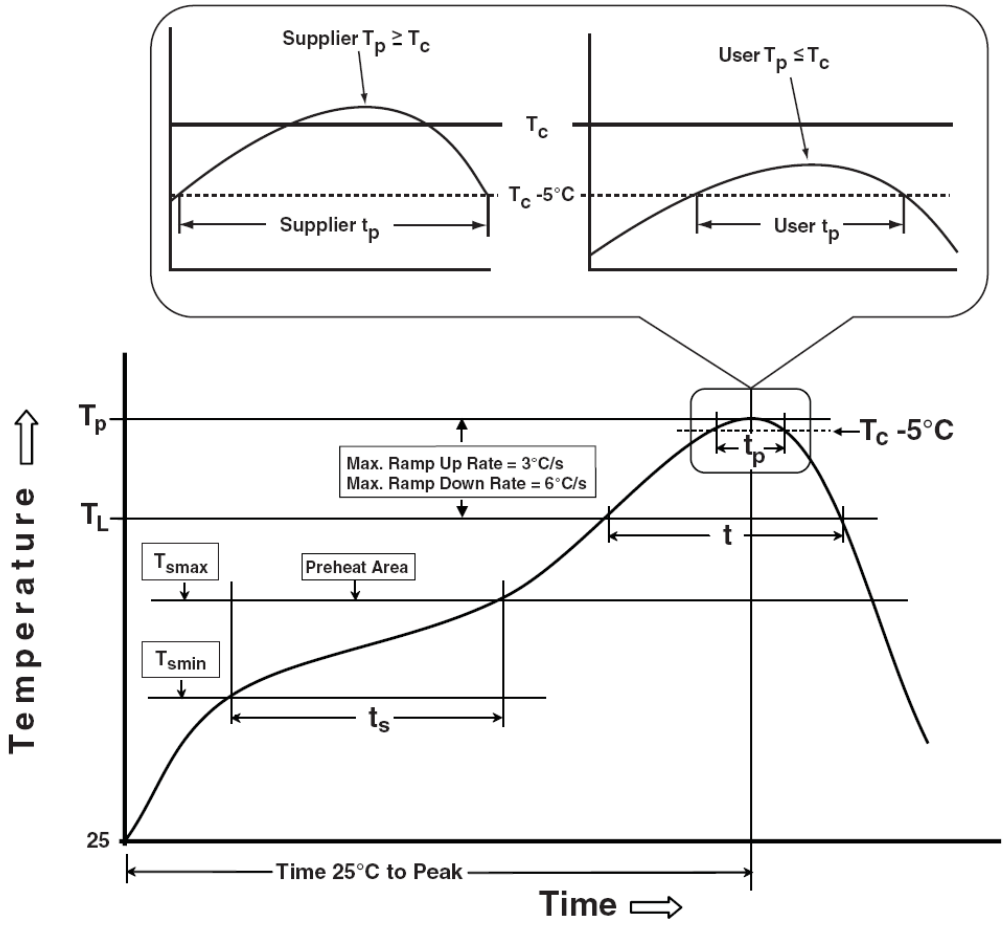
TQFN4x4-24A



TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_J=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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