PT1502

PMU for Portable Applications

GENERAL DESCRIPTION

The PT1502 is a integrated power management unit for small handheld portable applications. It contains a single-cell Lithium Ion battery charger, a synchronous step-down DC-DC converter and 2 Low Dropout Regulators. It allows charging from both wall adapter and USB port. When charging from wall adapter, the PT1502 increases the charging current automatically.

The battery charger is a highly integrated charging management device targeted at space limited portable applications. It offers an integrated MOSFET and current sensor, reverse blocking protection, high accuracy current and voltage regulation, charge status indication, and charge termination. It charges a battery in three phases: trickle charging, constant current, and constant voltage. No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. The thermal feedback regulates the charging current to limit the chip temperature during high power operation or high ambient temperature to maximize the charge rate without risk of overheating. The charge voltage is fixed at 4.2V, and the charge current can be programmed externally with a single resistor. The PT1502 automatically terminates the charge cycle when the charge current drops to 1/10 the programmed value after the final float voltage is reached. The PT1502 automatically re-starts the charge if the battery voltage falls below an internal threshold.

The step-down converter is a high efficiency monolithic current mode synchronous buck regulator with a constant operation frequency. A main switch and a synchronous switch are integrated in PT1502, the device has high efficiency and no external Schottky diode needed. 100% duty cycle provides low dropout operation, extending battery life in portable systems. Automatic burst mode operation at light loads provides high efficiency. Internal 1.5MHz switching frequency allowing the use of small surface mount inductors and capacitors. The output voltage can be adjusted by external resistors.

The two low-dropout voltage regulators are designed for portable and wireless applications. It can provides better than 60dB PSRR at 1kHz. The output current can be up to 200mA. One regulator's output voltage is fixed at 3.0V, and the other one is adjusted to 2.5V,2.8V,3.0V,3.3V by two control pins.

FEATURES

- Integrated switch for USB/AC Adapter supply
- 120uA quiescent supply current(includes step-down DC-DC converters and two low dropout regulators)
- Integrated single-cell lithium ion battery charger
  - Auto thermal regulated
  - Charging current up to 800mA
  - Charging current adjusted by external resistor
- Integrated step-down DC-DC converter
  - Output voltage adjusted by external resistor
  - Output current up to 600mA
  - 1.5M Hz fixed switching frequency
  - Over-current and over-temperature protection
- Integrated two low dropout regulators
  - LDO1: output voltage 3.0V，up to 200mA output current
  - LDO2: output voltage optional for 2.5V/2.8V/3.0V/3.3V，up to 200mA output current
  - PSRR: 60dB@1k Hz
  - Over-current and over-temperature protection
- QFN20（4X4）package

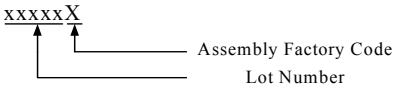
APPLICATIONS

- MP3/4
- PDAs
- GSM/CDMA mobile phone
- Portable media players

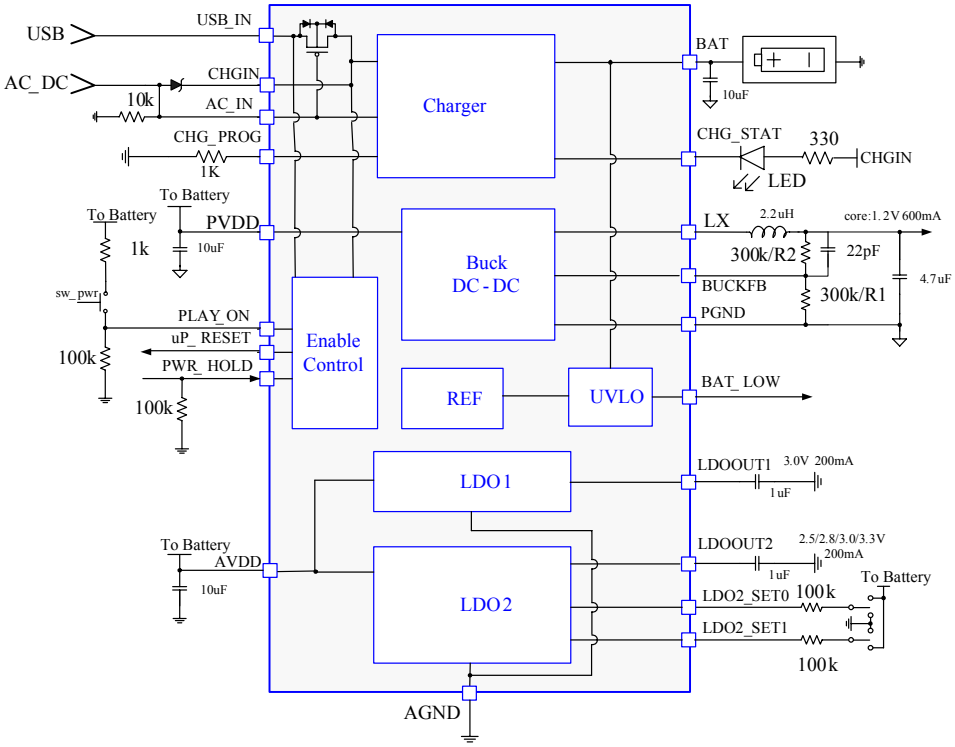
ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
QFN20	-40 °C to 85 °C	PT1502EQFN	Tape and Reel 3000 3000 units	PT1502 xxxxxX

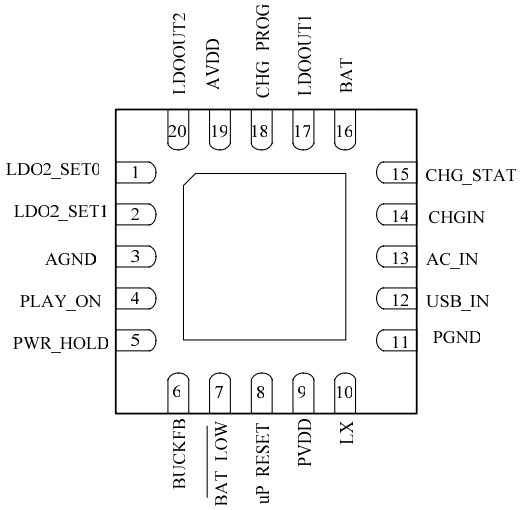
Note:



TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



PIN DESCRIPTION

PIN No.	PIN NAMES	PIN DESCRIPTION
1	LDO2_SET0	LDO2 output voltage setting bit，LSB
2	LDO2_SET1	LDO2 output voltage setting bit，MSB
3	AGND	Analog Ground
4	PLAY_ON	System start up signal for Battery
5	PWR_HOLD	feedback Chip enabled signal from CPU
6	BUCKFB	Feedback port for step-down DC-DC converter
7	BAT_LOW	Battery voltage lower than 3.3V signal
8	uP_RESET	CPU RESET signal
9	PVDD	supply port for step-down DC-DC converter
10	LX	Switch port for step-down DC-DC converter
11	PGND	Power Ground
12	USB_IN	USB supply
13	AC_IN	Indicator for AC Adapter connected
14	CHGIN	AC Adapter input
15	CHG_STAT	Indicator for charging status，Open-drain output
16	BAT	Battery input
17	LDOOUT1	LDO1 output
18	CHG_PROG	Charging current setting pin, connects resistor to AGND
19	AVDD	Analog supply
20	LDOOUT2	LDO2 output

ABSOLOUTE MAXIMUM RATING **(Note1)**

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	Input supply voltage: USB_IN，CHGIN，AVDD，PVDD	– 0.3 ~ 6	V
V_{IO}	Input/Output signal: PLAY_ON，PWR_HOLD，uP_RESET，BAT_LOW，LDO2_SET0，LDO2_SET1，BUCKFB，LDO1OUT，LDO2OUT，CHG_PROG，CHG_STAT，LX，AC_IN	– 0.3 ~ V_{IN}	V
T_J	Junction Temperature	-40~125	°C
T_{STG}	Storage Temperature Range	– 65 ~ 150	°C
T_{SOLDER}	Lead Temperature (Soldering, 10 sec)	260	°C

RECOMMENDED OPERATING RANGE(Note2)

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	Input supply voltage: USB_IN，CHGIN	4.25 ~ 5.5	V
V_{IN2}	Input supply voltage: AVDD，PVDD	3.5 ~ 5.5	V
T_{OPER}	Operating Temperature Range	– 40 ~ 85	°C
θ_{JA}	Thermal Resister	50	°C/W

Note1: Absolute Maximum Ratings are those values beyond which the life of the device maybe impaired.
Note2: Recommended operating Range indicates conditions for which the device is functional, but does not guarantee specific performance limits.

ELECTRICAL CHARACTERISTICS

（V_B=3.6V，T_A=25℃, unless otherwise specified）

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_Q	Bat supply quiescent current	CHGIN/USB_IN floating，BUCK/LDO1/LDO2 no load		120	300	μA
I_{SHDN}	Bat supply Shut down current	CHGIN/USB_IN floating，PLAY_ON=AGND, PWR_HOLD=AGND		1	5	μA
V_{IL}	Maximum Low Input Level at PLAY_ON, PWR_HOLD	AVDD = 3.0 to 5.5V			0.4	V
V_{IH}	Minimum High Input Level at PLAY_ON, PWR_HOLD	AVDD = 3.0 to 5.5V	1.4			V
V_{LBAT}	Battery voltage Undervoltage lockout threshold	VBAT high to low	3.135	3.3	3.465	V
T_{LBAT}	Battery voltage Undervoltage lockout comparator filter time			1		ms
$V_{LBATHYS}$	Battery voltage Undervoltage lockout hysteresis			100		mV
TSD	Thermal shutdown Temperature			160		°C
	Thermal shutdown Hysteresis			20		°C

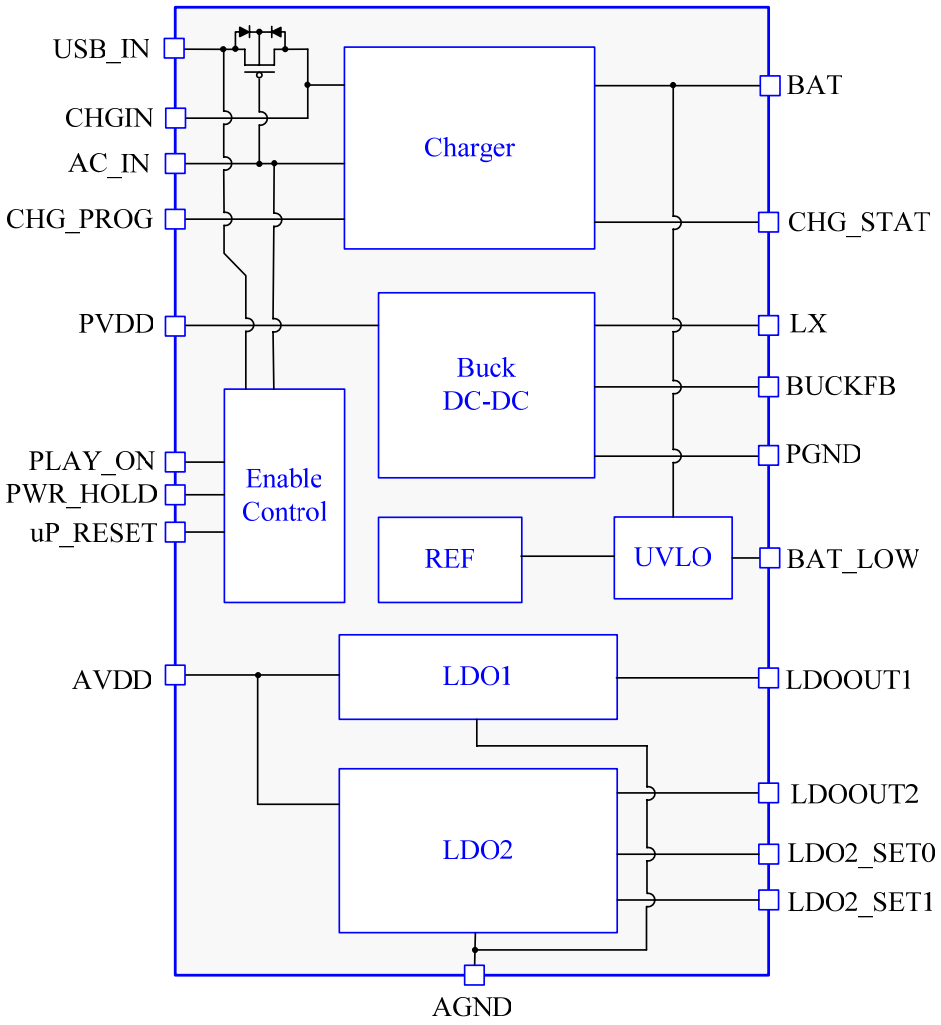
ELECTRICAL CHARACTERISTICS (continued)

Charger Characteristics						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{CHG}	Input Charging Supply Voltage		4.25		5.5	V
V_{BAT_REG}	Regulated Output Voltage	I_{CH_CC} = 50mA, R_{PROG} =5K	4.158	4.2	4.242	V
I_{CH_CC}	Const current mode Charging current	R_{PROG} =1K, USB mode	445	470	495	mA
		R_{PROG} =1K, Adapter mode		750		mA
I_{TRIKL}	Trickle Charge Current	$V_{BAT} < V_{TRIKL}$		I_{CH_CC}/10		mA
V_{TRIKL}	Trickle Charge Threshold Voltage	V_{BAT} from low to high		2.9		V
V_{TRHYS}	Trickle Charge Hysteresis Voltage			80		mV
V_{UV}	Under voltage Lockout Threshold	V_{CHGIN} from high to low		3.8		V
V_{UVHYS}	Under voltage Lockout Hysteresis			200		mV
I_{TERM}	Charging termination current			I_{CH_CC}/10		mA
V_{PROG}	CHG_PROG pin voltage	Const current mode		1.0		V
$I_{\overline{CHG\_TAT}}$	CHG_STAT Pin Weak Pull-Down Current	$V_{\overline{CHG\_STAT}}$ = 5V		20		μA
$V_{\overline{CHG\_TAT}}$	CHG_STAT Pin Output Low Voltage	$I_{\overline{CHG\_STAT}}$ = 5mA		0.35		V
ΔV_{RECHG}	Recharge Battery Threshold Voltage	V_{BAT_REG} - V_{CHG}		150		mV
T_{LIM}	Junction Temperature in Constant Temperature Mode			120		℃
T_{RECHG}	Recharge Comparator Filter Time	V_{BAT} from high to low		2		ms
I_{PROG}	PROG Pin Pull-Up Current			3		μA
DC-DC step down converter Characteristics						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{FB}	Regulated Feedback Voltage		0.588	0.600	0.612	V
ΔV_{OUT}	Line Regulation	PVDD = 3.5V to 5.5V		0.04	0.4	%/V
I_{LIMIT}	Peak Inductor Current			1		A
$V_{LOADREG}$	Load Regulation			0.5		%
F_{OSC}	Oscillator Frequency		1.2	1.5	1.8	MHz
R_{PFET}	RDS(ON) of P-Channel FET	I_{LX} = 100mA		0.4	0.5	Ω
R_{NFET}	RDS(ON) of N-Channel FET	I_{LX} = –100mA		0.35	0.45	Ω

ELECTRICAL CHARACTERISTICS (continued)

Low Dropout Regulator Characteristics							
SYMBOL	**PARAMETER**	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**UNITS**
V_{LDO1}	Output voltage 1				2.94	3.0	3.06	V
V_{LDO2}	Output voltage 2	LDO2_SET0=Low, LDO2_SET1=Low			2.45	2.5	2.55	V
		LDO2_SET0=High, LDO2_SET1=Low			2.744	2.8	2.856	
		LDO2_SET0=Low, LDO2_SET1=High			2.94	3.0	3.06	
		LDO2_SET0=High, LDO2_SET1=High			3.234	3.3	3.366	
ΔV_{OUT}	Line Regulation Error	AVDD=($V_{LDO(nom)}$ + 0.5V) to 5.5V				0.1	0.5	%/V
	Load Regulation Error	I_{LDO_OUT} = 1mA to 150 mA				15	50	mV
I_{OUTMAX}	Peak Output Current	$V_{LDO} \geq V_{LDO(nom)} - 2\%$				300		mA
PSRR	Power Supply Rejection Ratio	AVDD = $V_{LDO(nom)}$+1.0V	f = 1k Hz	I_{OUT} = 50mA		60		dB
				I_{OUT} = 150mA		60		
			f = 10k Hz	I_{OUT} = 50mA		55		
				I_{OUT} = 150mA		55		
V_{DIFF}	Dropout Voltage	I_{LDO_OUT} = 50mA				50	90	mV
		I_{LDO_OUT} = 100mA				100	180	mV
I_{SC}	Output Short Current Limit	Output Grounded				500		mA
ΔV_{LDO_OUT}/ V_{OUT}	V_{OUT} Temperature Characteristics	Temperature = -40 to 125°C				100		ppm/°C

SIMPLIFIED BLOCK DIAGRAM



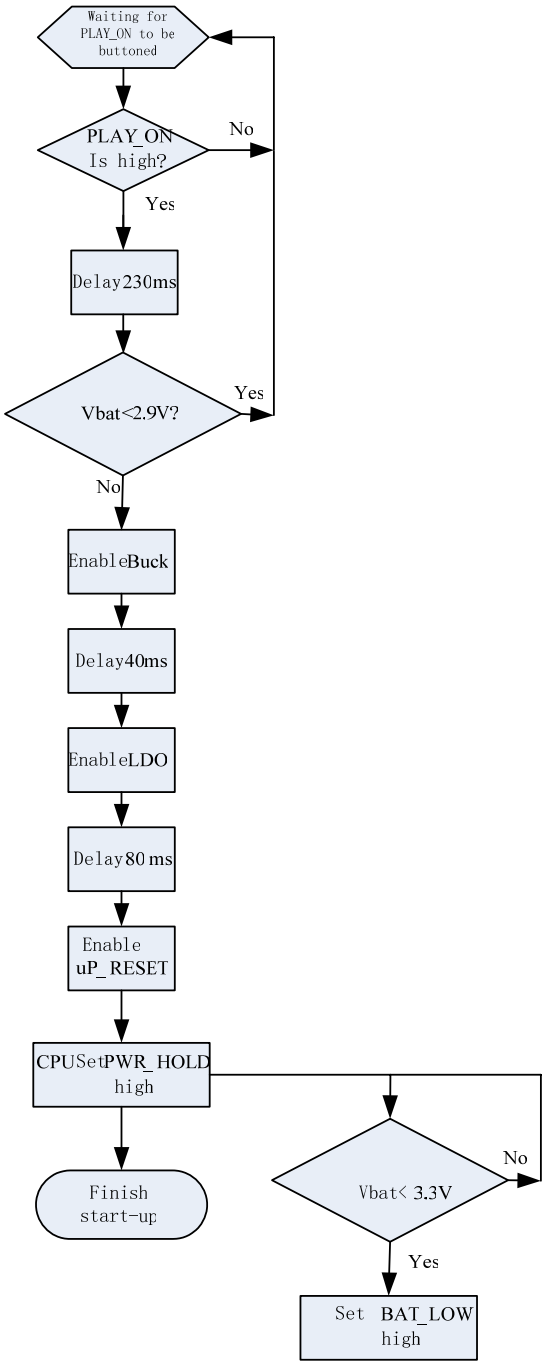
Operation Description

Power up sequency:

The uP_RESET signal will reset the CPU. And the PWR_HOLD contains the PMU in normal working status.

When the PLAY_ON button is hold up to high level for several hundred milliseconds， PMU will be ready to start. First, to start the Buck, then delay 40 milliseconds, to start the LDO, and after 80 milliseconds, the uP_RESET turns on to high level.

Start up sequence by external button：



Power Down Description：

When button the PLAY_ON in working status, this action will be checked by CPU, and it shuts up inner blocks and sends low level to PWR_HOLD. When the PLAY_ON is loosened the PLAY_ON becomes low, and PMU will power down.

Bat Low Voltage Detection：

When in working status, the voltage of Bat pin lowers than 3.3V, then PT1502 puts the BAT_LOW pin to high level. This signal will be sent to CPU.

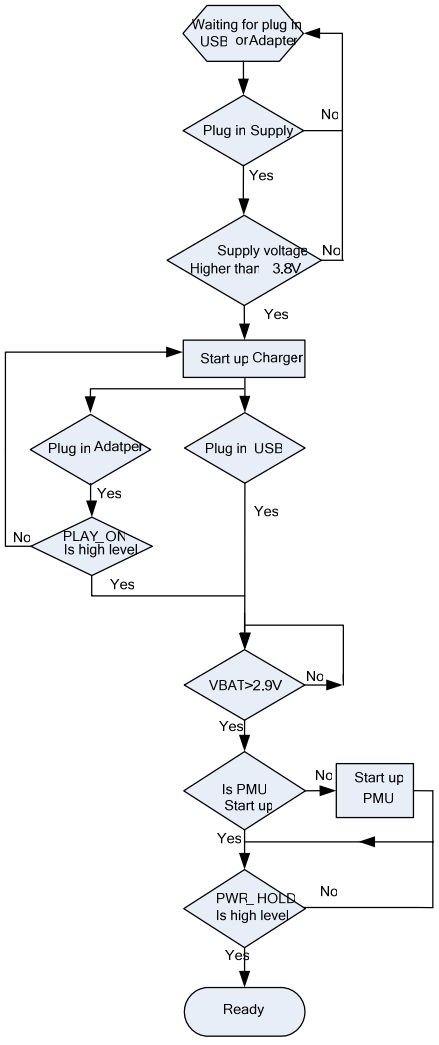
Adapter and USB plug in：

When USB or Adapter is plugged in, the PT1502 would detect whether the supply is higher than 3.8V. If the supply voltage is lower than 3.8V, the charger stops to charge.

And if the Battery voltage is lower than 2.9V, PMU doesn't start up. And it will charge the battery until it over the 2.9V.

When the battery is absent, the PT1502 will stabilize the BAT pin voltage to 4.2V.

Sequence of plugging in the USB or Adapter：



Battery Charger

The PT1502 includes a linear Li-ion battery charger with thermal regulation. With the internal 0.6 ohms MOSFET, the minimum charging supply voltage can be less than 4.25V. One external 1% precision resistor is required to set the charging current value. When the voltage at the CHGIN pin rises above the UVLO threshold, the normal charging cycle begins. If the battery voltage is less than 2.9V, the device will operate in a trickle charging mode. The charging current in the trickle charging mode is $1/10^{th}$ of the programmed value, which effectively protects the battery from damage and prolongs its lifetime. When the voltage at the BAT pin rises above 2.9V, the charger enters the constant-current mode in which case the charging current equals to the programmed value. Once the voltage at the BAT pin reaches 4.2V, the charger goes into the constant voltage mode where the charging current decreases. Once the charging current drops to $1/10^{th}$ the programmed value, the charging cycle ends.

After a charge cycle is complete and the charging operation is terminated, the PT1502 keeps monitoring the BAT voltage. It will recharge the battery as soon as the BAT voltage drops below 4.05V. The PT1502 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When the PROG pin is floating, the charger goes into the shutdown mode.

BUCK

The PT1502 includes a high efficiency current mode synchronous buck regulator with a constant operation frequency. Its internal integrated MOSFETs achieve high efficiency. Ultra low output voltages are easily available with the 0.6V feedback reference voltage. Internal fixed 1.5MHz switching frequency allowing the use of small surface mount inductors and capacitors. The 2.7V to 5.5V input voltage range and 600mA output current make the BUCK ideally suited for single Li-Ion battery-powered applications.

Current Mode PWM Control Loop

Slope compensated current mode PWM control and cycle-by-cycle current limit provides stable operation and excellent line and load regulation. During normal operation, the internal top power MOSFET is turned on each cycle when the rising edge of the oscillator sets the RS latch, and turned off when rising edge of the PWM comparator resets the RS latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse or the beginning of the next clock cycle. The internal comparator controls output transient overshoots is smaller than 8% by turning the main MOSFET off until the fault is removed.

Skip-Cycles Mode Operation

At light loads, the BUCK enters skip-cycle mode automatically. In this mode, the inductor current may reach zero or reverse on each cycle. The PWM control loop will automatically skip cycles to maintain output regulation. The bottom MOSFET is turned off by the current reversal comparator, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator.

Low-Dropout Operation

When the input voltage deceases to the value of output voltage, the control loop remains the main MOSFET on until it reaches 100% duty cycle. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. Caution must be exercised to ensure the heat dissipated not to exceed the maximum junction temperature of the IC because the RDSON of the main MOSFET increases and the efficiency of the converter decrease.

LDO

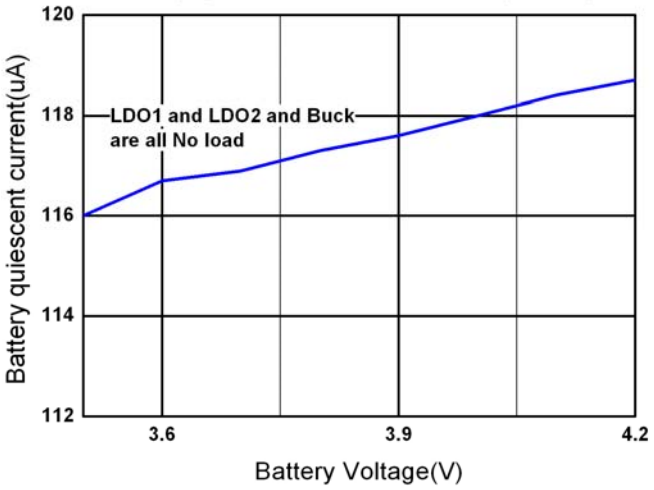
The block of Voltage Reference provides the reference voltage of the LDO.

The op-amp block is used as the error amplifier of the LDO by comparing the reference with the output feedback voltages. Its output controls the gate of a large PMOS pass element and hereby adjusts the output voltage.

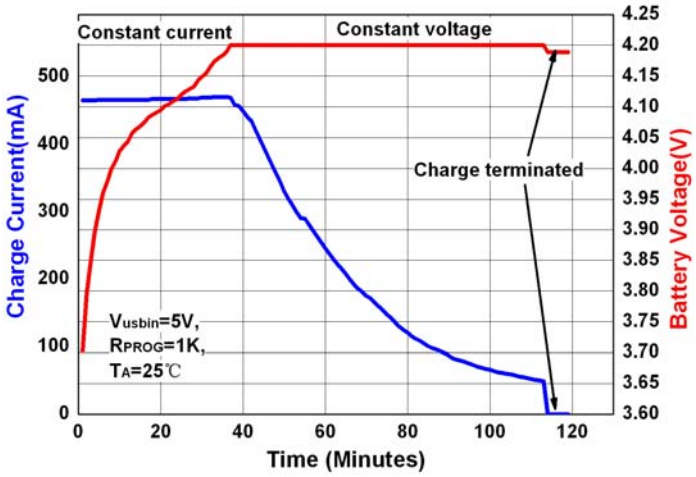
The Current Limit block senses the LDO output current and limits the output current from being too high. This is mostly a short circuit protection feature.

TYPICAL PERFORMANCE CHARACTERISTICS

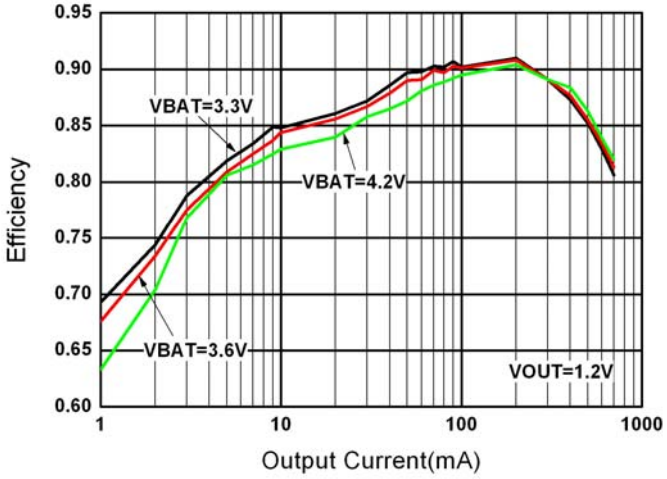
Battery quiescent current Vs Battery Voltage



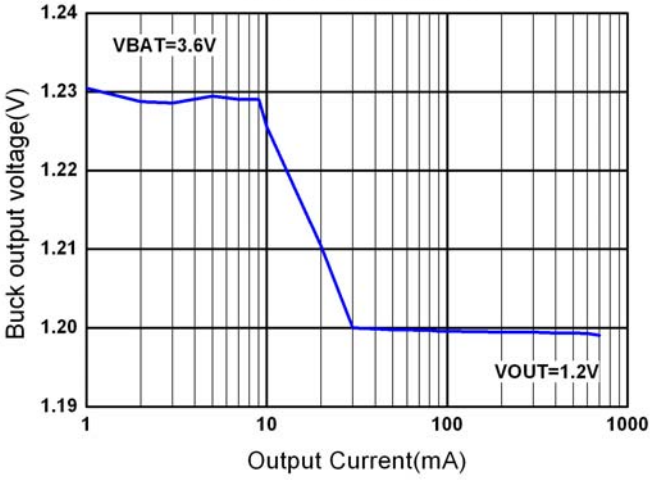
Complete Charging Cycle(900mAh Battery)



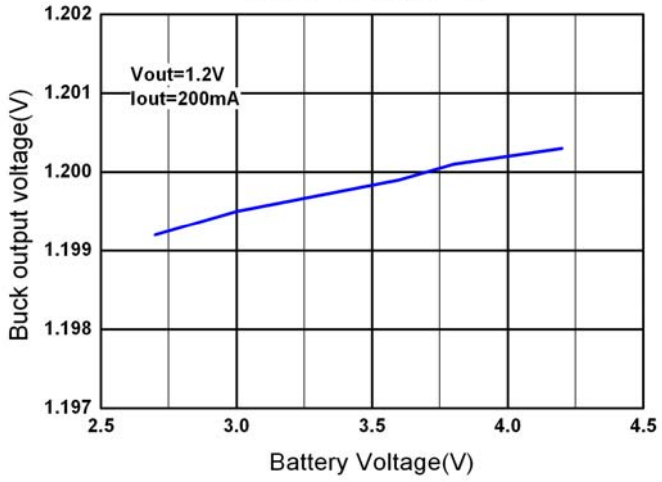
Buck Efficiency Vs Output Current



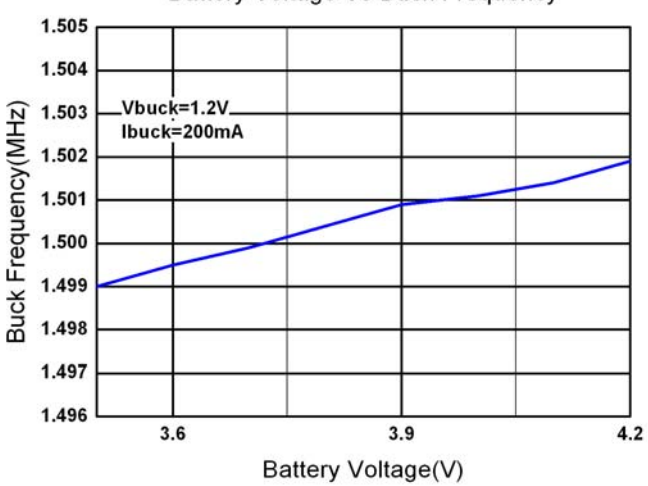
Buck Load Regulation

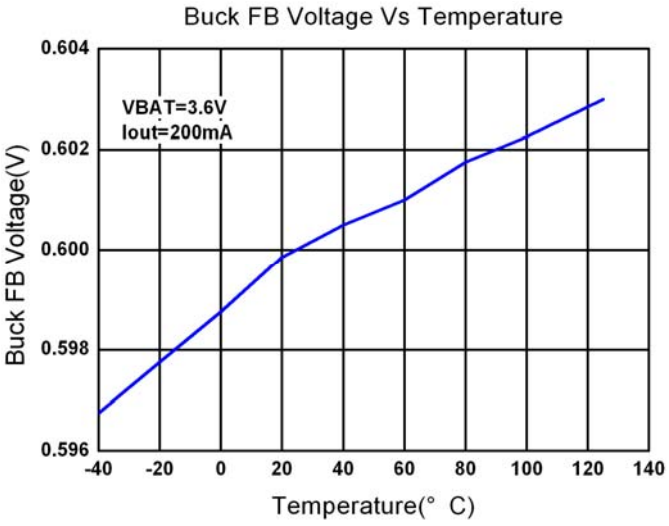


Buck Line Regulation

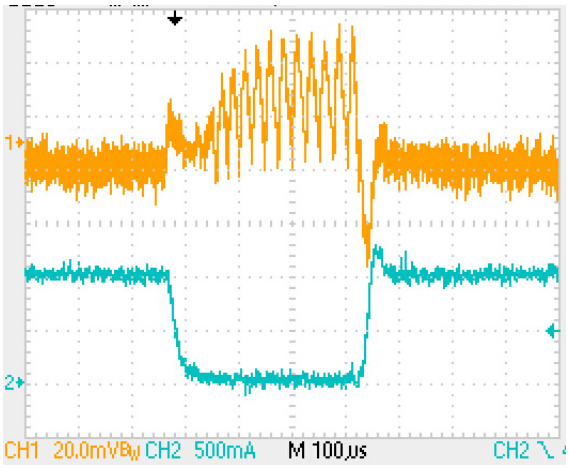


Battery Voltage Vs Buck Frequency



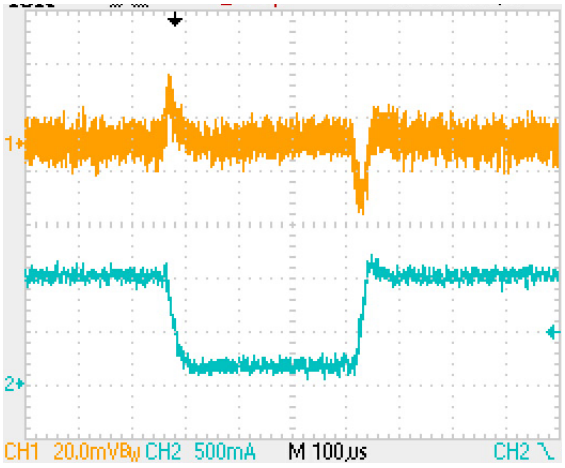


Buck Load Transient Response (Ibuck=10mA to 600mA, VBAT=3.6V, Vbuck=1.2V,Cout=4.7uF)

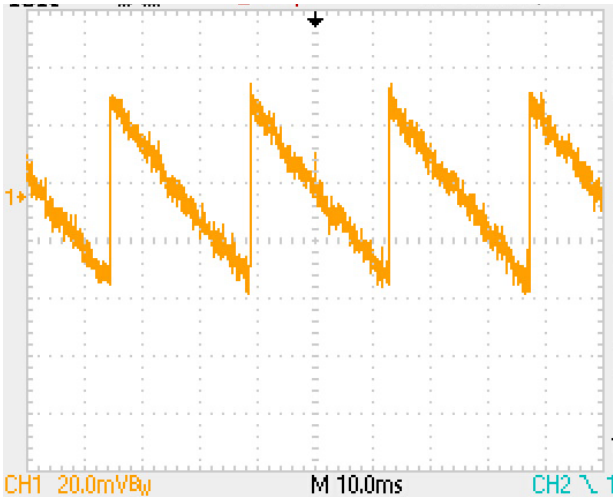


Buck Load Transient Response (Ibuck=10mA to 200mA, VBAT=3.6V, Vbuck=1.2V,Cout=4.7uF)

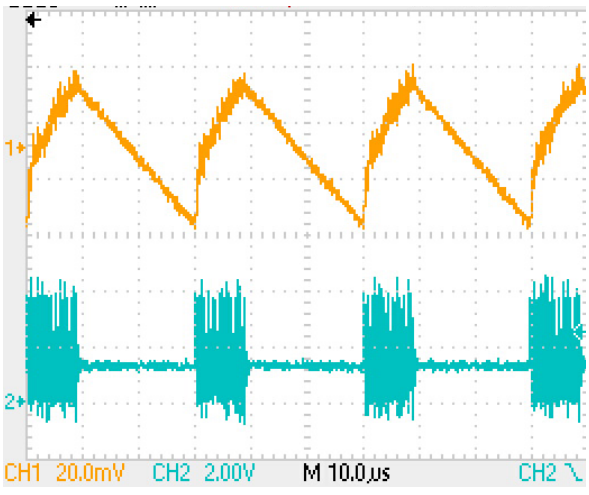
Buck Load Transient Response (Ibuck=100mA to 600mA, VBAT=3.6V, Vbuck=1.2V,Cout=4.7uF)



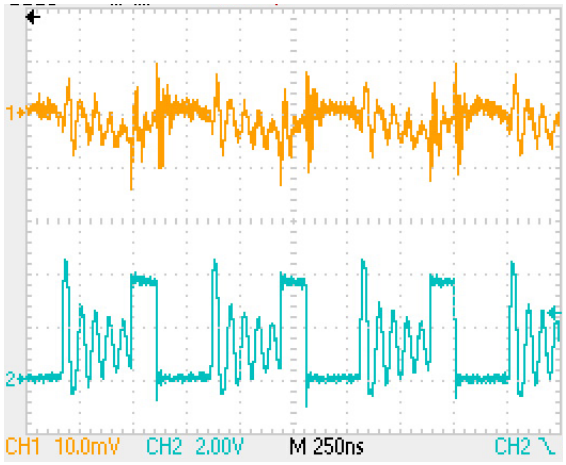
Buck No Load Output Voltage Ripple (VBAT=3.6V, Vbuck=1.2V,Cout=4.7uF)



Buck Output Voltage Ripple Vs LX (VBAT=3.6V, Ibuck=10mA,Vbuck=1.2V,Cout=4.7uF)



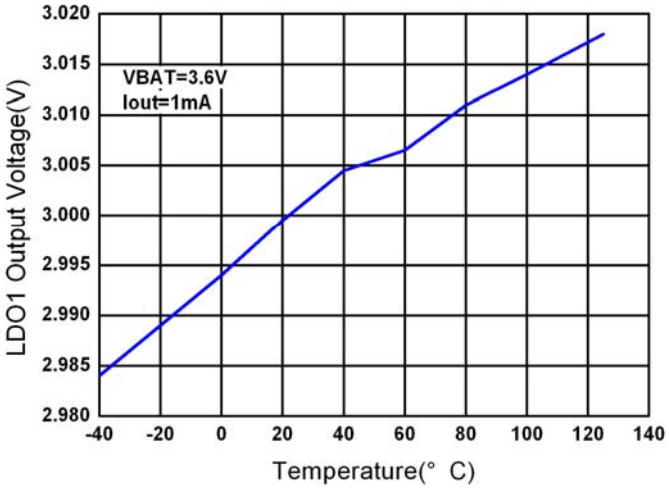
Buck Output Voltage Ripple Vs LX (VBAT=3.6V, Ibuck=40mA,Vbuck=1.2V,Cout=4.7uF)



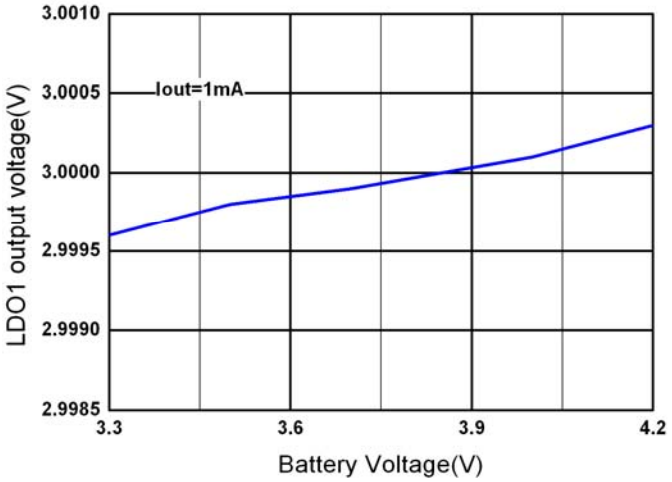
Buck Output Voltage Ripple Vs LX (VBAT=3.6V, Ibuck=200mA,Vbuck=1.2V,Cout=4.7uF)

Buck Output Voltage Ripple Vs LX (VBAT=3.6V, Ibuck=600mA,Vbuck=1.2V,Cout=4.7uF)

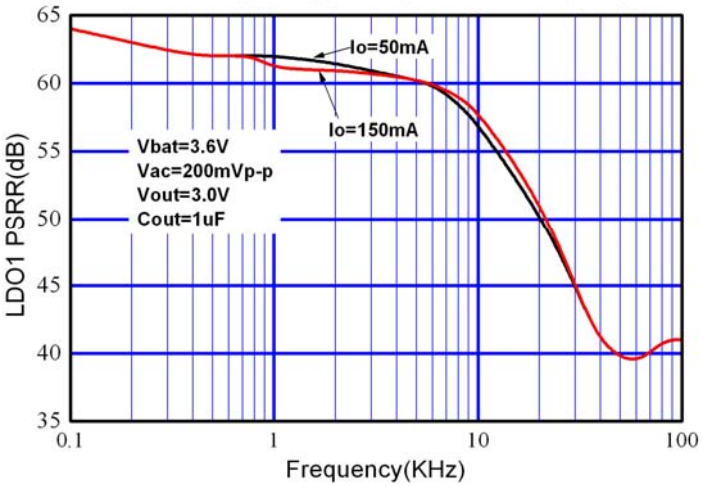
LDO1 Output Voltage Vs Temperature

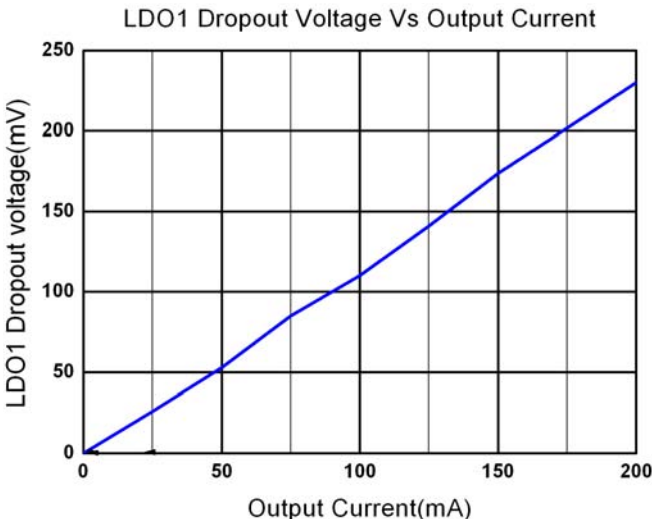


LDO1 Line Regulation

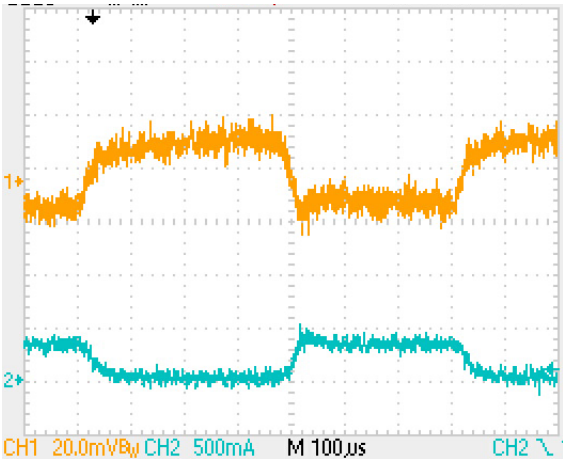


LDO1 Power Supply Ripple Rejection vs. Frequency

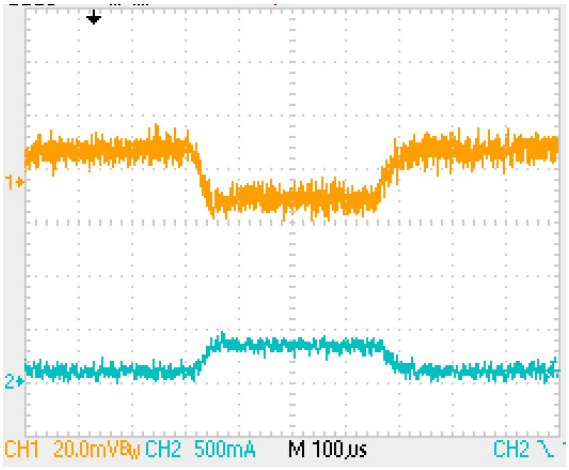




LDO1 Load Transient Response (ILDO1=0mA to 200mA, VBAT=3.6V,Cldo1_out=1uF)



LDO1 Load Transient Response (ILDO1=50mA to 200mA, VBAT=3.6V,Cldo1_out=1uF)



APPLICATION INFORMATION

Battery Charger

Adjusting Charging Current

The charging current is programmed using 1% precision resistor from PROG pin to ground. When USB supply the PT1502, the charging current and the programming resistor are calculated using the following equations:

R_{PROG}=470V/I_{CHG}, I_{CHG}=470V/R_{PROG}

When Adapter alone or both Adapter and USB supply the PT1502, the charging current and the programming resistor are calculated using the following equations:

R_{PROG}=750V/I_{CHG}, I_{CHG}=750V/R_{PROG}

Charge status indicator

The charging status indicator pin has three different states: strong pull down(about 10mA current sink), weak pull down(about 20µA current sink), and high impedance. The strong pull down mode indicates the PT1502 is in a charging cycle. A weak pull down mode indicates the CHGIN reaches the UVLO and the charger is ready to charge. The high impedance indicates the PT1502 is in Under Voltage Lock Out (UVLO) mode. A microprocessor can distinguish the three states.

Thermal limiting

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 120℃. This feature protects the PT1502 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the PT1502.

The conditions that cause the PT1502 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET—this is calculated to be approximately:

$PD = (V_{CHGIN} - V_{BAT}) \bullet I_{BAT}$

Where PD is the power dissipated

V_{CHGIN} is the input supply voltage

V_{BAT} is the battery voltage

I_{BAT} is the charge current.

The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$T_A = 120℃ - PD \bullet \theta_{JA}$

$T_A = 120℃ - (V_{CHGIN} - V_{BAT}) \bullet I_{BAT} \bullet \theta_{JA}$

Reducing the voltage drop across the internal MOSFET can significantly decrease the power dissipation in the IC. This has the effect of increasing the current delivered to the battery during thermal regulation. One method is by dissipating some of the power through an external component, such as a resistor or diode. By dropping voltage across a resistor in series with a 5V wall adapter, the on-chip power dissipation can be decreased, thus increasing the thermally regulated charge current.

Under Voltage Lockout (UVLO)

An internal under voltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until CHGIN rises above the under voltage lockout threshold. The UVLO circuit has a built-in hysteresis of 200mV. Furthermore, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if CHGIN falls to within 30mV of the battery voltage. If the UVLO comparator is tripped, the charger will not come out of shutdown mode until V_{CHGIN} rises 100mV above the battery voltage.

Stability Considerations

The constant-voltage mode feedback loop is stable without an output capacitor provided a battery is connected to the charger output. With no battery present, an output capacitor is recommended to reduce ripple voltage. In constant current mode, the PROG pin is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the PROG pin. With no additional capacitance on the PROG pin, the charger is stable with the programming resistor value as high as 20k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz.

BUCK

Setting the Output Voltage

The output voltage is set by an external resister divider according to the following formula:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R2}{R1}\right)$$

Inductor Selection

For most applications, the PT1502 operates well with inductors of 1uH to 4.7uH. Low inductance values are physically smaller but require fast switching, which results in efficiency loss. The inductor value can be calculated from following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Table 1 list some typical surface mount inductors that adapt to PT1502 applications

Part #	L (μH)	Max DCR (mΩ)	Rated D.C. Current (A)	Size WxLxH (mm)
Sumida CR43	1.4 2.2 3.3 4.7	56.2 71.2 86.2 108.7	2.52 1.75 1.44 1.15	4.5x4.0x3.5
Sumida CDRH4D18	1.5 2.2 3.3 4.7	75 110 162	1.32 1.04 0.84	4.7x4.7x2.0
Toko D312C	1.5 2.2 3.3 4.7	120 140 180 240	1.29 1.14 0.98 0.79	3.6x3.6x1.2

Table 1. Typical Surface Mount Inductors

Input and Output Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

Ceramic capacitor with X5R or C7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 4.7uF ceramic capacitor for most applications is sufficient.

The output capacitor is required to obtain small output voltage ripple and ensure regulation loop stability. Typically, once the ESR requirement for COUT has been met, the RMS current generally far exceeds the ripple current requirement. The output ripple △VOUT is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \times (ESR + \frac{1}{8 f C_{OUT}})$$

Where f is the operating frequency, COUT is the output capacitor and △IL is the ripple current of inductor current.

Ceramic capacitors with X5R or C7R dielectrics are recommended due to their low ESR and high current rating. A 10uF ceramic capacitor for most applications is recommended for low output voltage ripple and good loop stability.

LDO

Input Capacitor

An input capacitor of ≥ 1.0μF is required between the AVDD and GND pin. This capacitor must be located within 1cm distance from AVDD pin and connected to a clear ground. A ceramic capacitor is recommended although a good quality tantalum or film may be used at the input. However, a tantalum capacitor can suffer catastrophic failures due to surge current when connected to a low impedance power supply (such as a battery or a very large capacitor).

There is no requirement for the ESR on the input capacitor, but the tolerance and temperature coefficient must be considered in order to ensure the capacitor work within the operation range over the full range of temperature and operating conditions.

Output Capacitor

In applications, it is important to select the output capacitor to keep the PT1502 in stable operation. The output capacitor must meet all the requirements specified in the following recommended capacitor table over all conditions in applications. The minimum capacitance for stability and correct operation is 0.6μF. The capacitance tolerance should be ±30% or better over the operation temperature range. The recommended capacitor type is X7R to meet the full device temperature specification.

Recommended Output Capacitor (C_{OUT})

	TYP	MIN	MAX	Unit
Capacitance	1.0	0.6	10	μF
ESR		0	400	mΩ

The capacitor application conditions also include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below minimum specified value.

The LDO is designed to work with very small ceramic output capacitors. A 1.0μF capacitor (X7R type) with ESR type between 0 and 400mΩ is suitable in the PT1502 applications. X5R capacitors may be used but have a narrow temperature range. With these and other capacitor types (Y5V, Z6U) that may be used, selection relies on the range of operating conditions and temperature range for a specified application.

It may also be possible to use tantalum or film capacitors at the output, but these are not as good for reasons of size and cost.

It is also recommended that the output capacitor be located within 1cm from the output pin and return to a clean ground wire.

NO-LOAD Stability

The LDO will remain stable and in regulation with no external load. This is especially important in CMOS RAM keep-alive applications.

LDO Output voltage setting:

LDO2_SET0	LDO2_SET1	LDO2OUT
Low	Low	2.5V
High	Low	2.8V
Low	High	3.0V
High	High	3.3V

The table of voltage of LDO2 setting

The voltage of LDO1is fixed at 3.0V。

The voltage of LDO2 can be adjusted to 2.5V，2.8V，3.0V，3.3V by setting LDO2_SET0 and LDO2_SET1.

Layout Guideline

Below figure is the schematic for the DEMO board. The DEMO board has extra components for easy evaluation. When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the PT1502:

1. The exposed pad must be reliably soldered to PGND/AGND and multilayer GND. The exposed thermal pad should be connected to board ground plane. The ground plane should include a large exposed copper pad under the package with VIAs to all board layers for thermal dissipation.

2. The power traces, including GND traces, the LX traces and the PVDD trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several via pads when routing between layers.

3. The input capacitors should be connected as close as possible to CHGIN and PGND to get good power filtering.

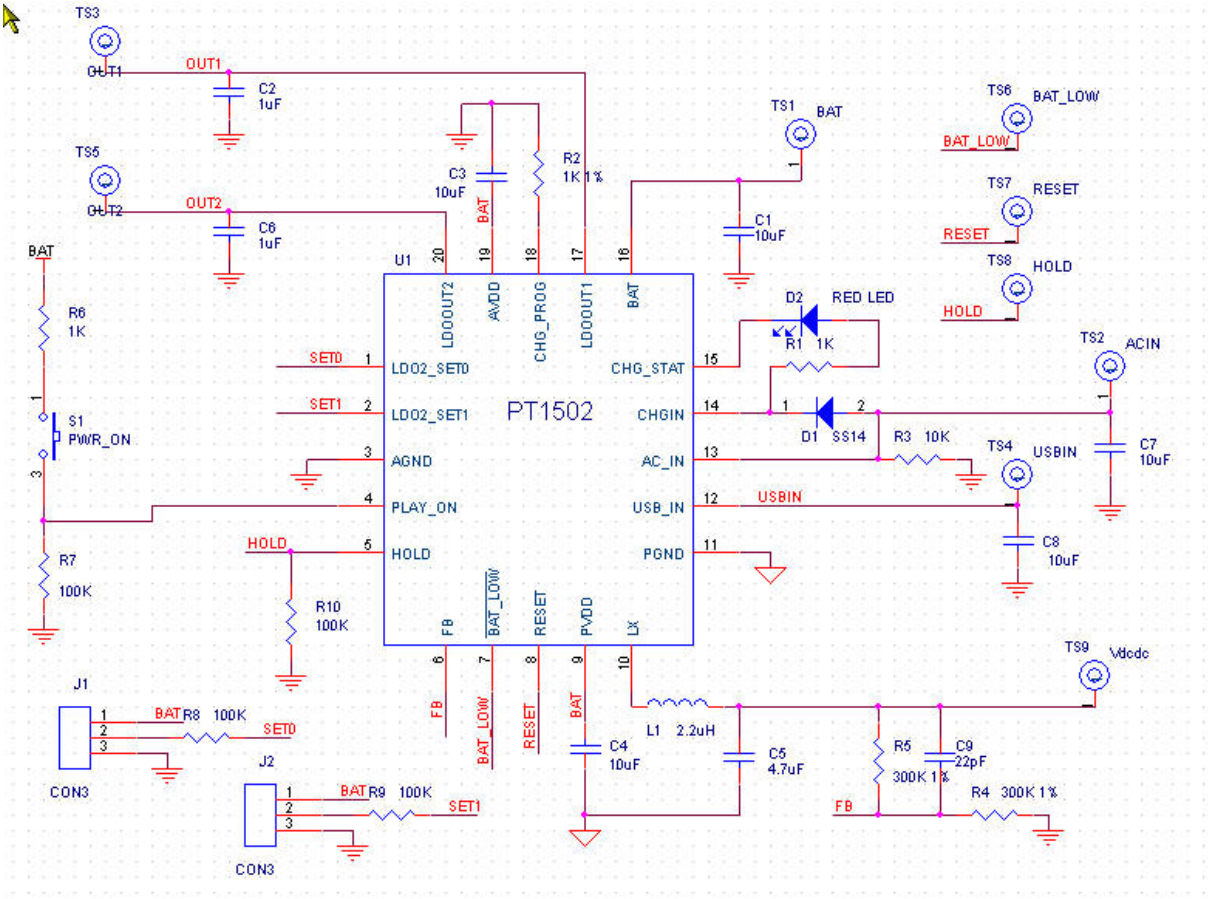
4. Keep the switching node LX away from the sensitive FB node.

5. The feedback trace for the BUCK should be separate from any power trace and connected as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation.

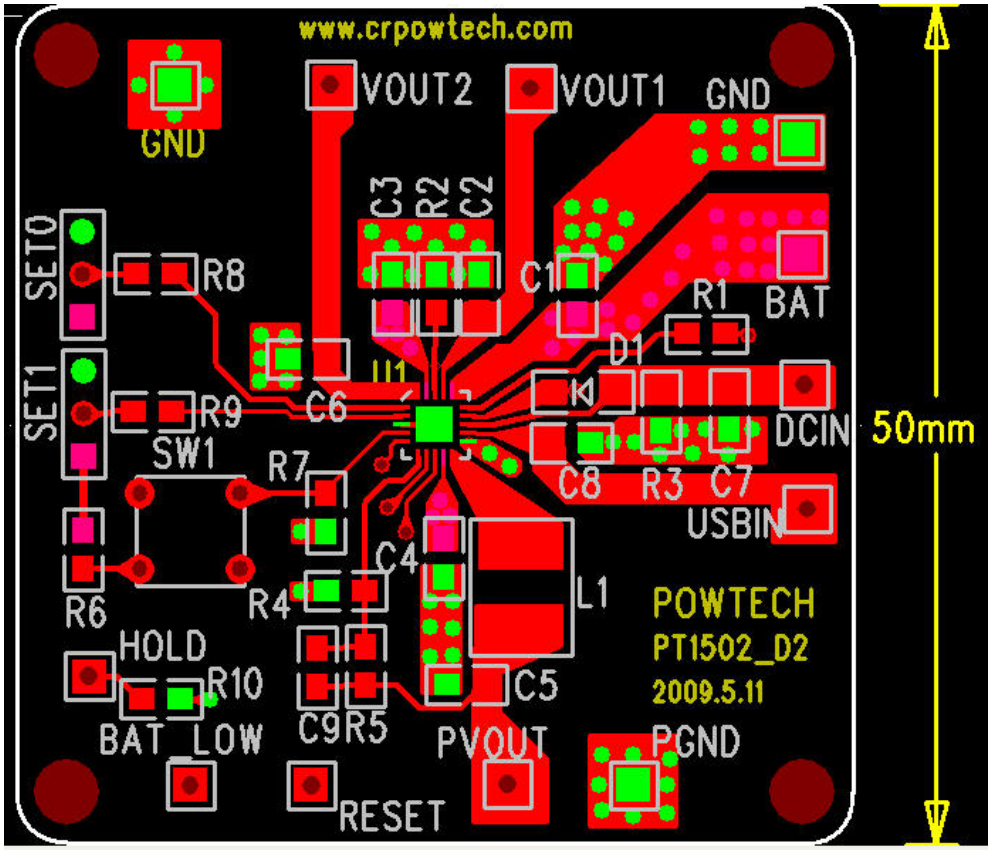
6. The output capacitor and L1 should be connected as close as possible and there should not be any signal lines under the inductor.

7. The resistance of the trace from the load return to the PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

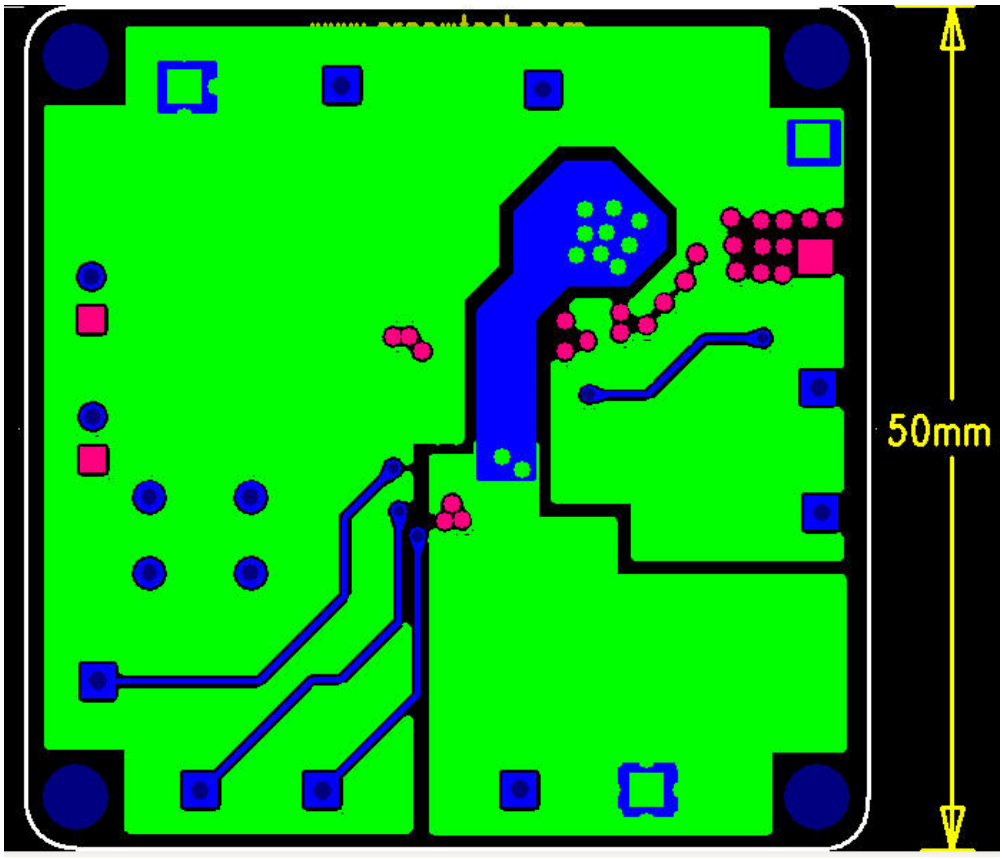
The schematic of the DEMO Board



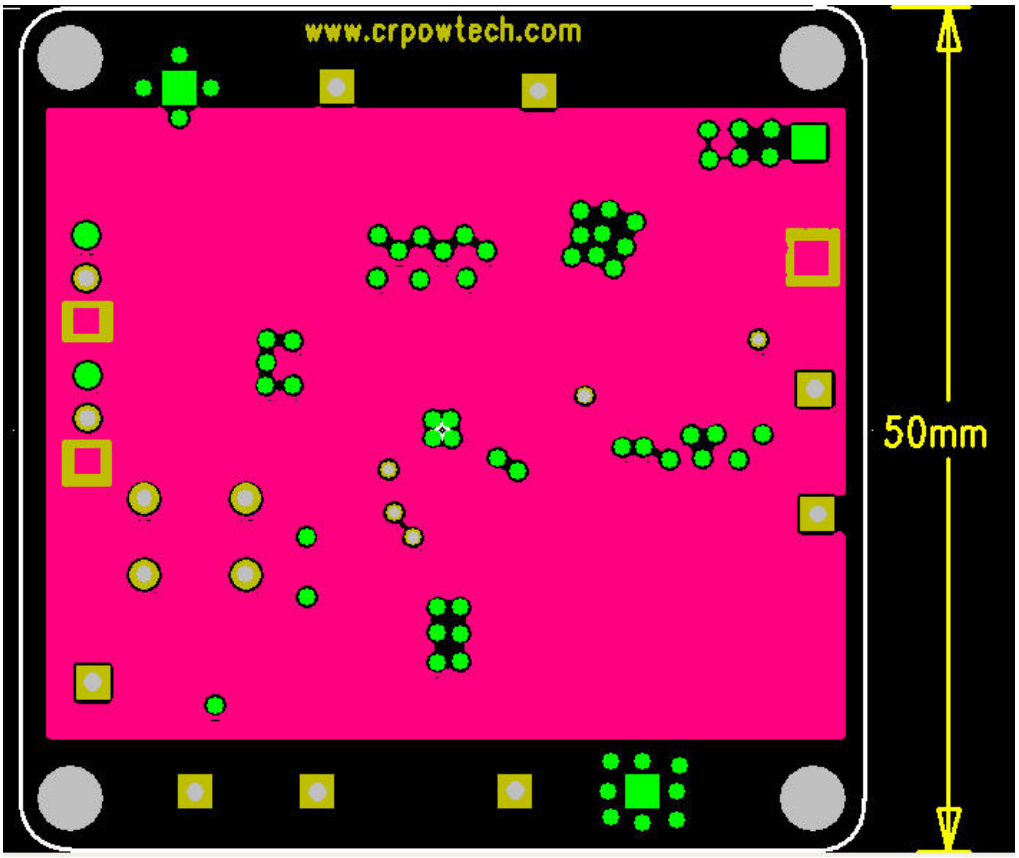
The Top layer of the DEMO board



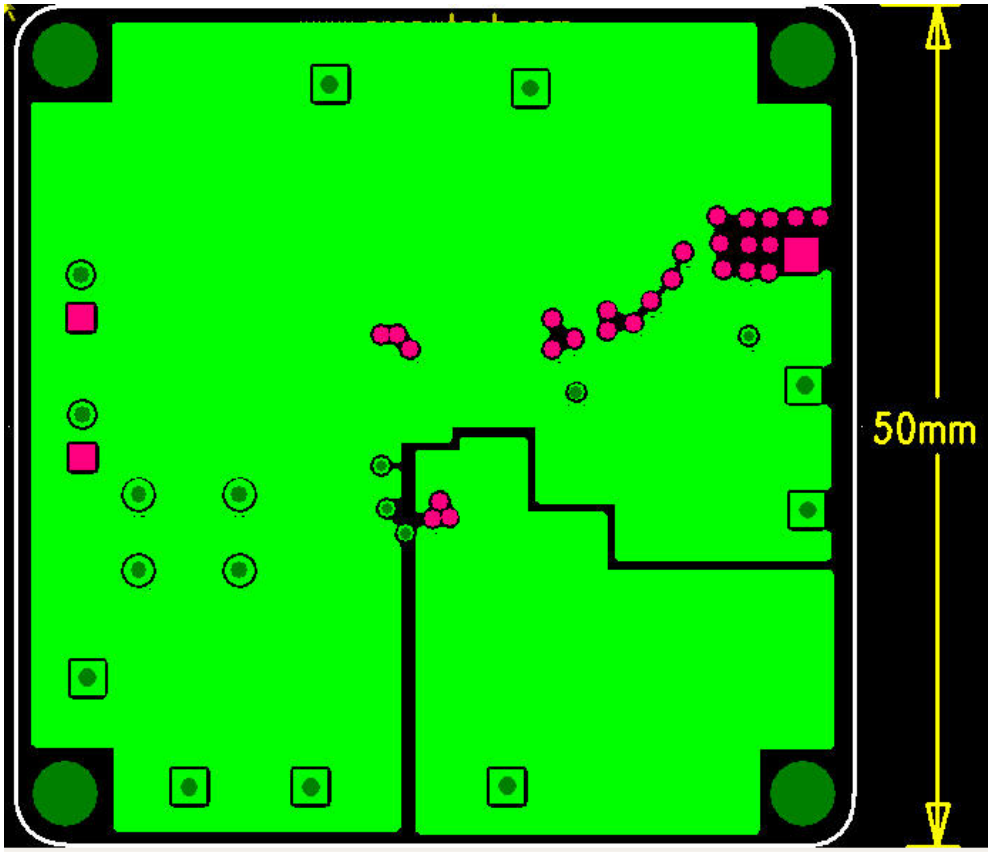
The Bottom layer of the DEMO board



The Power layer of the DEMO board

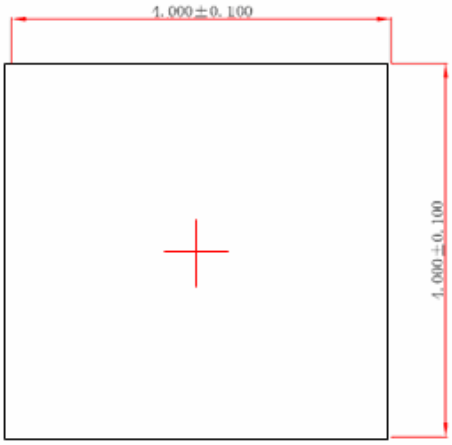


The GND layer of the DEMO board

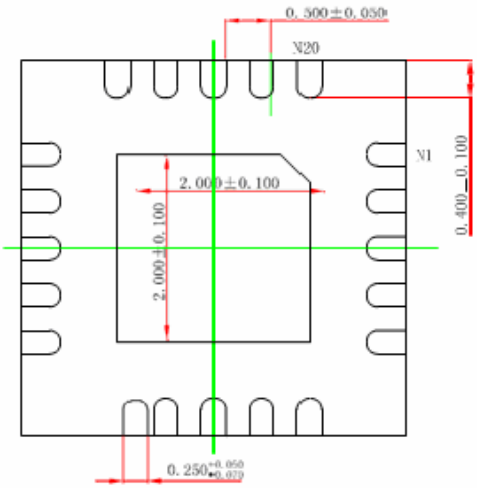


PACKAGE INFORMATION

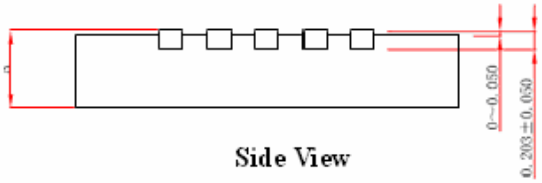
QFN20(4*4)



Top View



Bottom View



Side View