CSD87501L 30 V Dual Common Drain N-Channel NexFET™ Power MOSFET

1 Features

- Low On-Resistance
- Small Footprint of 3.37 × 1.47 mm
- Ultra-Low Profile – 0.2 mm High
- Pb-Free
- RoHS Compliant
- Halogen Free
- Gate ESD Protection

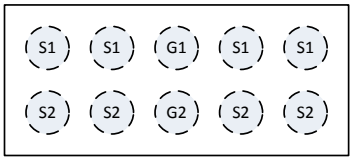
2 Applications

- Battery Management
- Battery Protection
- USB Type-C /PD

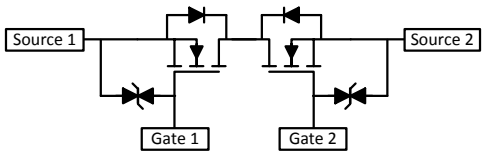
3 Description

This 30 V, 6.6 mΩ, 3.37 mm × 1.47 mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance and gate charge in a small footprint. Its small size and common drain configuration make the device ideal for multi-cell battery pack applications and small handheld devices.

Top View



Configuration



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{S1S2}	Source-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	15		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.0		nC
$R_{S1S2(on)}$	Source-to-Source On-Resistance	V_{GS} = 4.5 V	9.3	mΩ
		V_{GS} = 10 V	6.6	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information(1)

Device	Media	Qty	Package	Ship
CSD87501L	7-Inch Reel	3000	3.37 mm X 1.47 mm Land Grid Array Package	Tape and Reel
CSD87501LT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

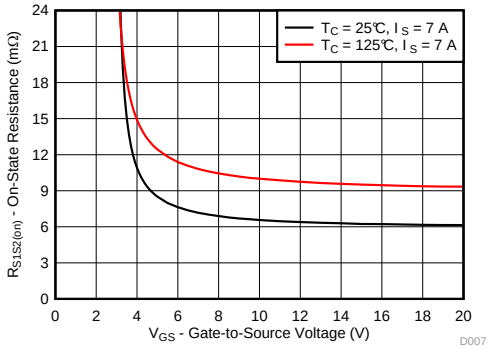
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_S	Continuous Source Current(1)	14	A
I_{SM}	Pulsed Source Current (2)	72	A
P_D	Power Dissipation	2.5	W
$V_{(ESD)}$ Rating	Human Body Model (HBM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

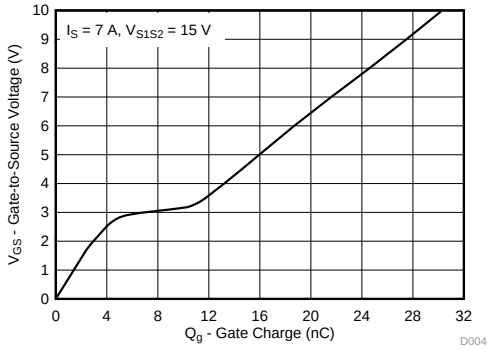
(1) Typical $R_{\theta JA}$ = 50°C/W on a 1 inch^2, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Typical min Cu $R_{\theta JA}$ = 135°C/W, pulse duration ≤100 µs, duty cycle ≤1%.

$R_{S1S2(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (February 2015) to Revision A **Page**

- Extended Y axis in Figure 9 down to 0.01 A ... 5

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-Source Voltage	V_{GS} = 0 V, I_S = 250 µA	30			V
I_{S1S2}	Source-to-Source Leakage Current	V_{GS} = 0 V, V_{S1S2} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{S1S2} = 0 V, V_{GS} = 20 V			10	µA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	1.3	1.8	2.3	V
$R_{S1S2(on)}$	Source-to-Source On-Resistance	V_{GS} = 4.5 V, I_S = 7 A		9.3	11.0	mΩ
		V_{GS} = 10 V, I_S = 7 A		6.6	7.8	mΩ
g_{fs}	Transconductance	V_{S1S2} = 3 V, I_S = 7 A		48		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{S1S2} = 15 V, f = 1 MHz		1620	2110	pF
C_{oss}	Output Capacitance			189	246	pF
C_{rss}	Reverse Transfer Capacitance			152	198	pF
R_G	Series Gate Resistance			300	450	Ω
Q_g	Gate Charge Total (4.5 V)	V_{S1S2} = 15 V, I_S = 7 A		15	20	nC
Q_g	Gate Charge Total (10 V)			31	40	nC
Q_{gd}	Gate Charge Gate-to-Drain			6.0		nC
Q_{gs}	Gate Charge Gate-to-Source			5.0		nC
$Q_{g(th)}$	Gate Charge at V_{th}			2.5		nC
Q_{oss}	Output Charge	V_{S1S2} = 15 V, V_{GS} = 0 V		7.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{S1S2} = 15 V, V_{GS} = 10 V, I_{S1S2} = 7 A, R_G = 0 Ω		164		ns
t_r	Rise Time			260		ns
$t_{d(off)}$	Turn Off Delay Time			709		ns
t_f	Fall Time			712		ns

(1) Dynamic characteristics values specified are per single FET.

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		135		°C/W
	Junction-to-Ambient Thermal Resistance(2)		50		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.

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5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

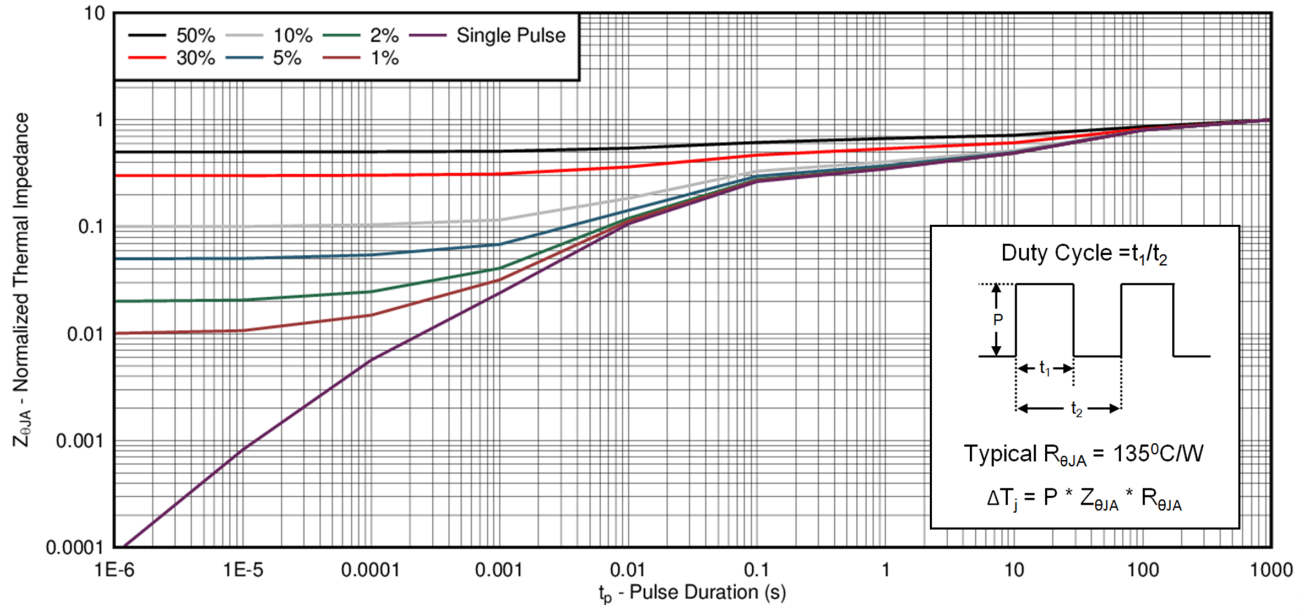

Figure 1. Transient Thermal Impedance

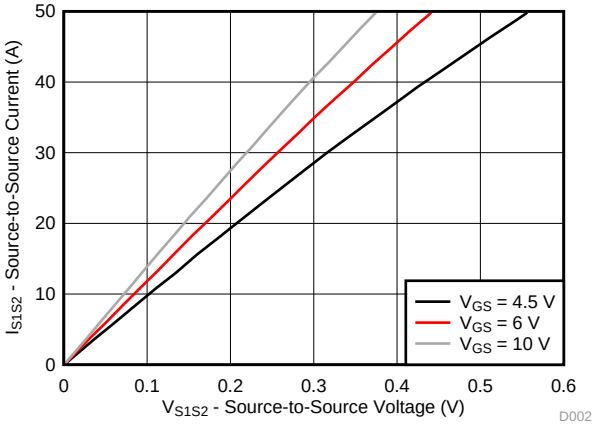

Figure 2. Saturation Characteristics

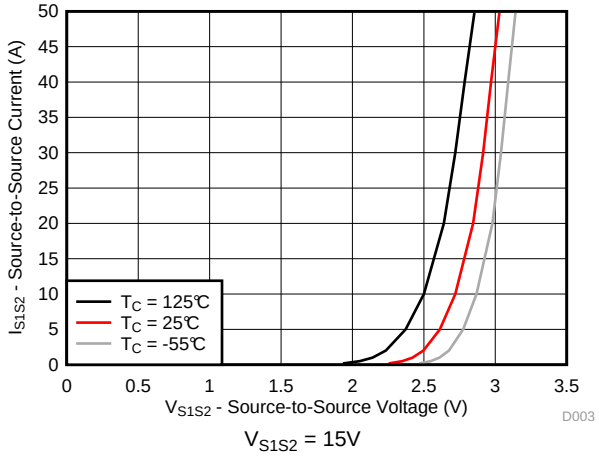

Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

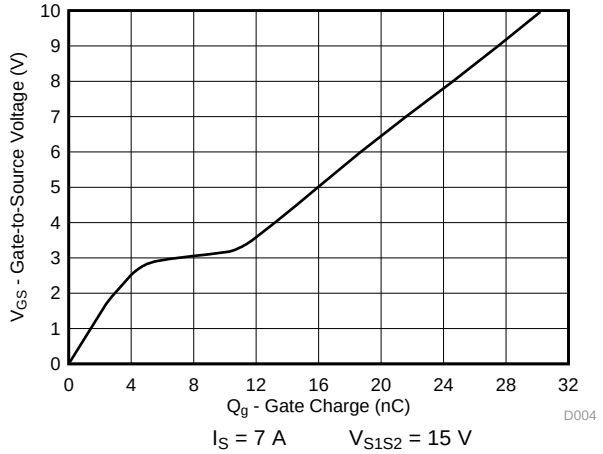

Figure 4. Gate Charge

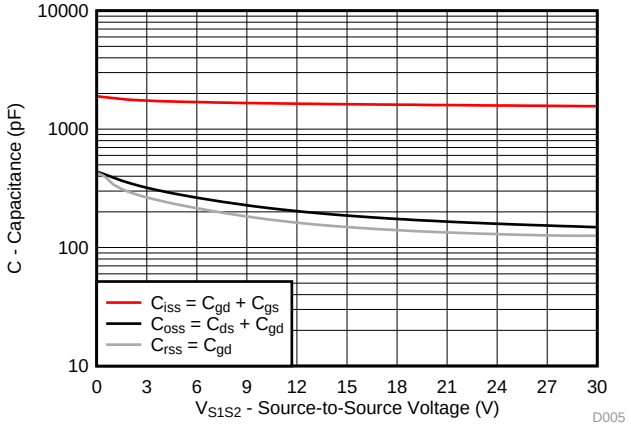

Figure 5. Capacitance

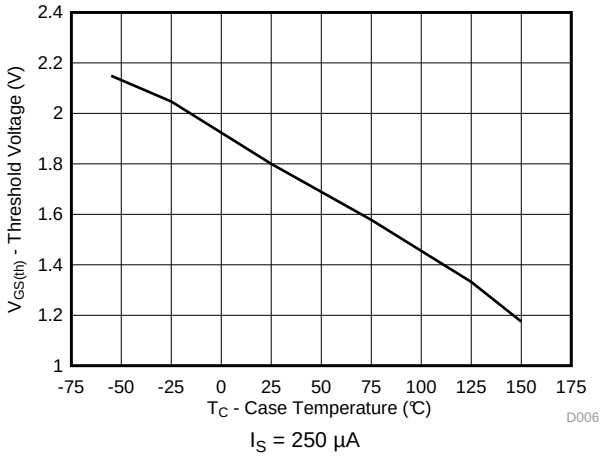

Figure 6. Threshold Voltage vs Temperature

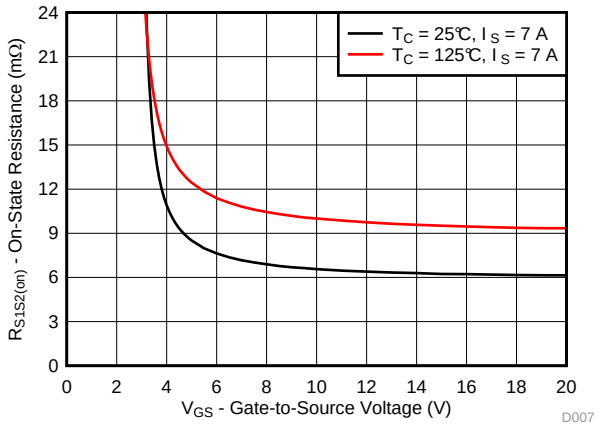

Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

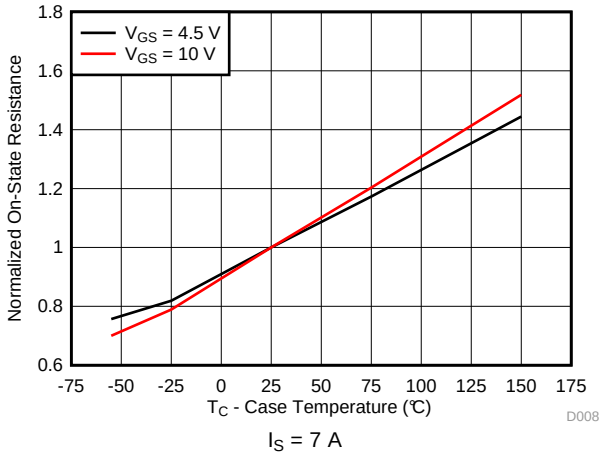

Figure 8. Normalized On-State Resistance vs Temperature

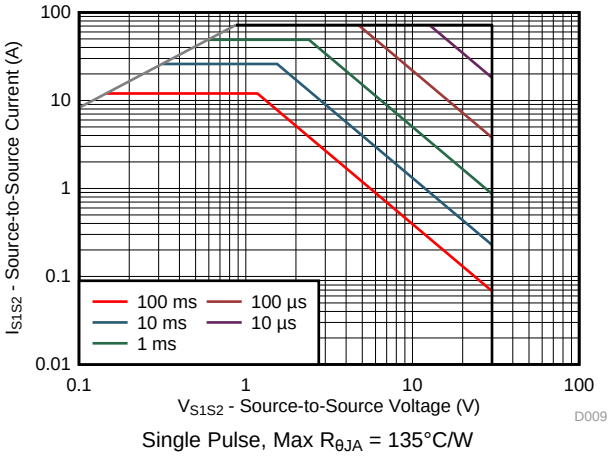

Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

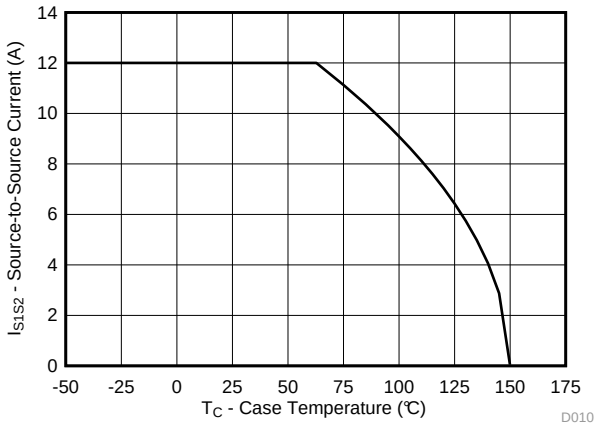

Figure 10. Maximum Source Current vs Temperature

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6 Device and Documentation Support

6.1 Trademarks

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6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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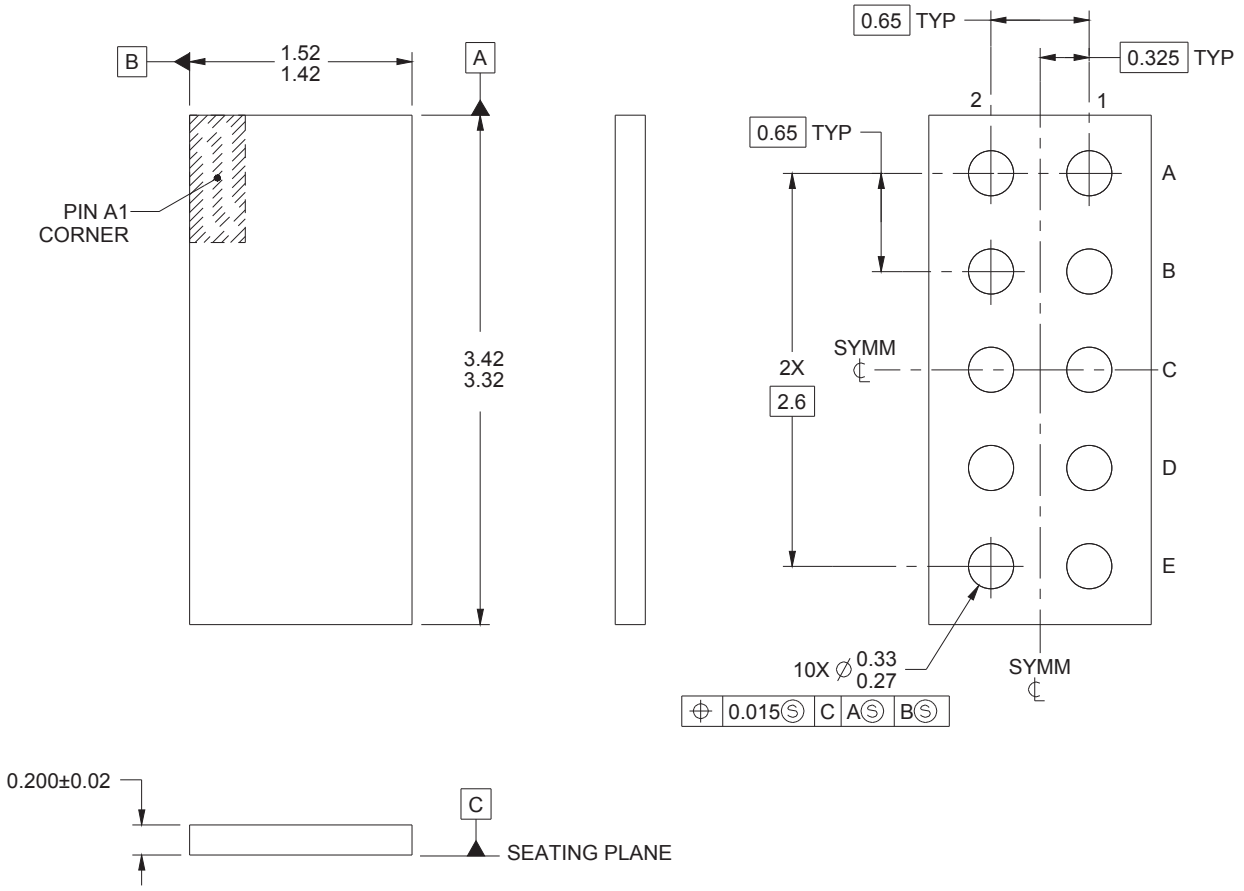
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions



All dimensions in millimeters.

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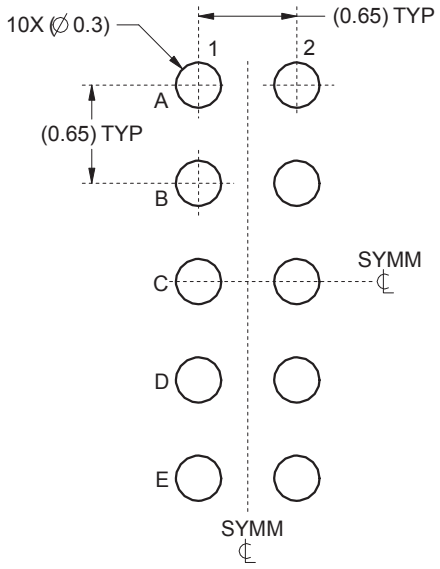
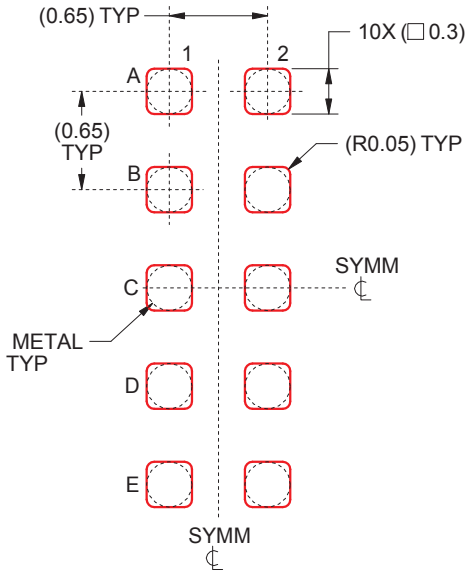
7.2 Recommended PCB Pattern



7.3 Recommended Stencil Pattern



All dimensions are in millimeters unless otherwise noted.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87501L	ACTIVE	PICOSTAR	YJG	10	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CSD87501	Samples
CSD87501LT	ACTIVE	PICOSTAR	YJG	10	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		CSD87501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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