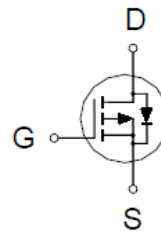


# PE551BA

## P-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
-30V	20m $\Omega$ @ $V_{GS} = -10V$	-22A



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 25$	
Continuous Drain Current <sup>3</sup>	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	-22	A
	$T_C = 100\text{ }^\circ\text{C}$		-14	
	$T_A = 25\text{ }^\circ\text{C}$		-7	
	$T_A = 70\text{ }^\circ\text{C}$		-5.8	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-40	
Avalanche Current		$I_{AS}$	-23	
Avalanche Energy	$L = 0.1\text{mH}$	$E_{AS}$	26	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	17	W
	$T_C = 100\text{ }^\circ\text{C}$		7	
	$T_A = 25\text{ }^\circ\text{C}$		1.9	
	$T_A = 70\text{ }^\circ\text{C}$		1.2	
Junction & Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

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## P-Channel Logic Level Enhancement Mode MOSFET

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$		65	°C / W
Junction-to-Case	$R_{\theta JC}$		7.2	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$ .

<sup>3</sup>Package limitation current is -21A.

### ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.6	-3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 25V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24V, V_{GS} = 0V$			-1	$\mu A$
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 55^\circ\text{C}$			-10	
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -7A$		15	20	m $\Omega$
		$V_{GS} = -4.5V, I_D = -7A$		23	30	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -10V, I_D = -7A$		25		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -15V, f = 1\text{MHz}$		1009		pF
Output Capacitance	$C_{oss}$			154		
Reverse Transfer Capacitance	$C_{rss}$			121		
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$		8		$\Omega$
Total Gate Charge <sup>2</sup>	$Q_g(V_{GS} = -10V)$	$V_{DS} = -15V, I_D = -7A$		21		nC
	$Q_g(V_{GS} = -4.5V)$			11		
Gate-Source Charge <sup>2</sup>	$Q_{gs}$			3		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$			6		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$		$V_{DD} = -15V,$ $I_D \cong -7A, V_{GS} = -10V, R_{GEN} = 6\Omega$		22	
Rise Time <sup>2</sup>	$t_r$			16		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$			50		
Fall Time <sup>2</sup>	$t_f$			25		

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**P-Channel Logic Level Enhancement Mode MOSFET**

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub> = 25 °C)**

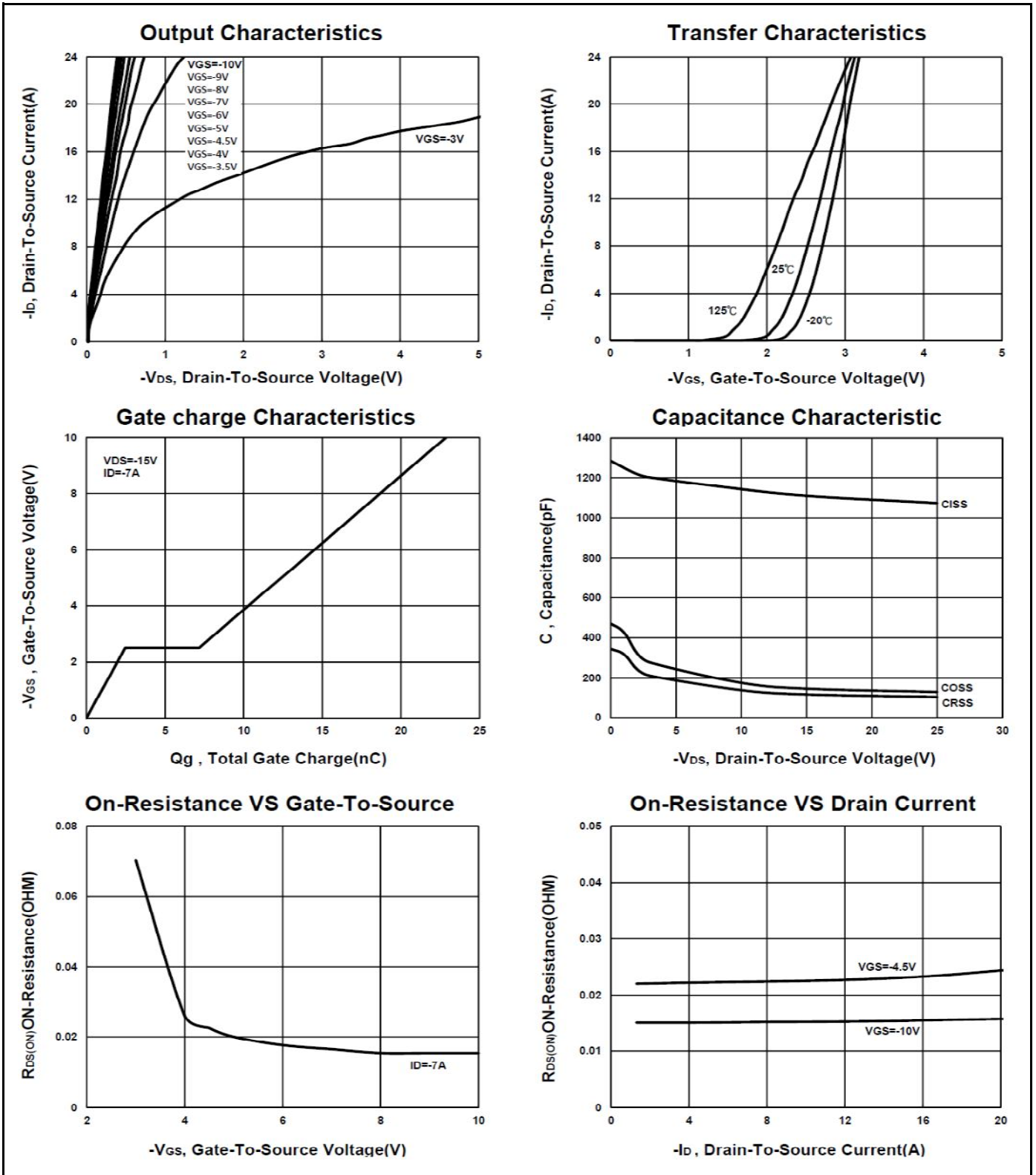
Continuous Current	I <sub>S</sub>				-13	A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = -7A, V <sub>GS</sub> = 0V			-1.3	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -7A, dI <sub>F</sub> /dt = 100A / μS		11		nS
Reverse Recovery Charge	Q <sub>rr</sub>			3		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

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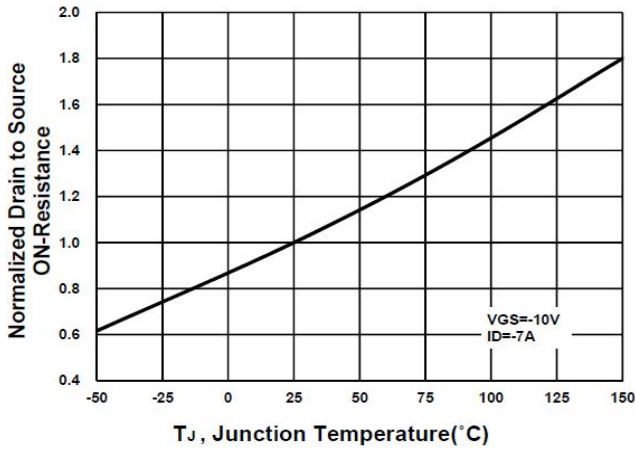
## P-Channel Logic Level Enhancement Mode MOSFET



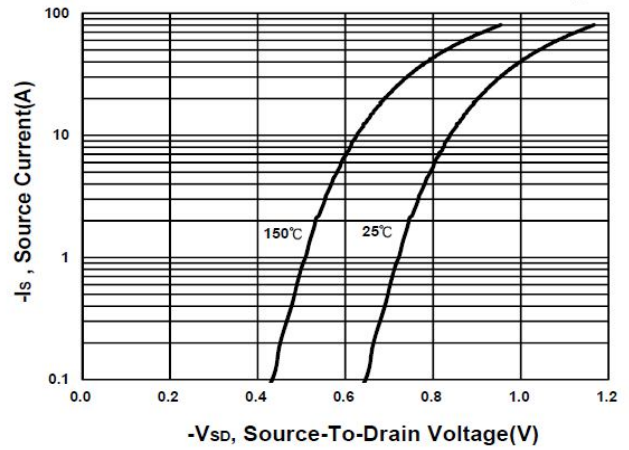
# PE551BA

## P-Channel Logic Level Enhancement Mode MOSFET

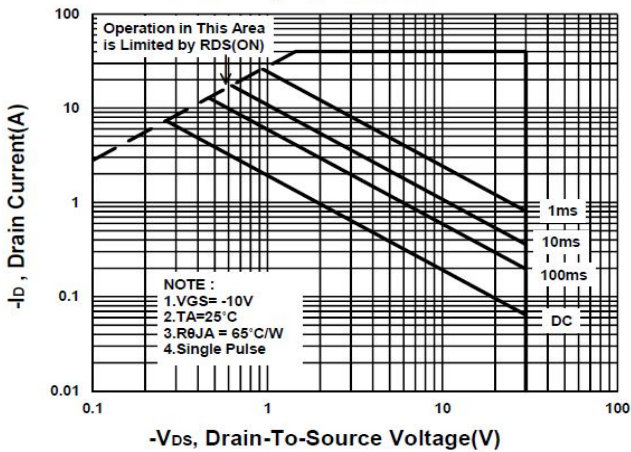
**On-Resistance VS Temperature**



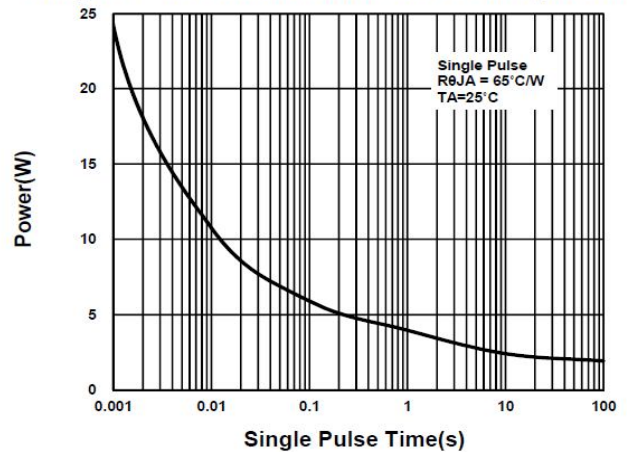
**Source-Drain Diode Forward Voltage**



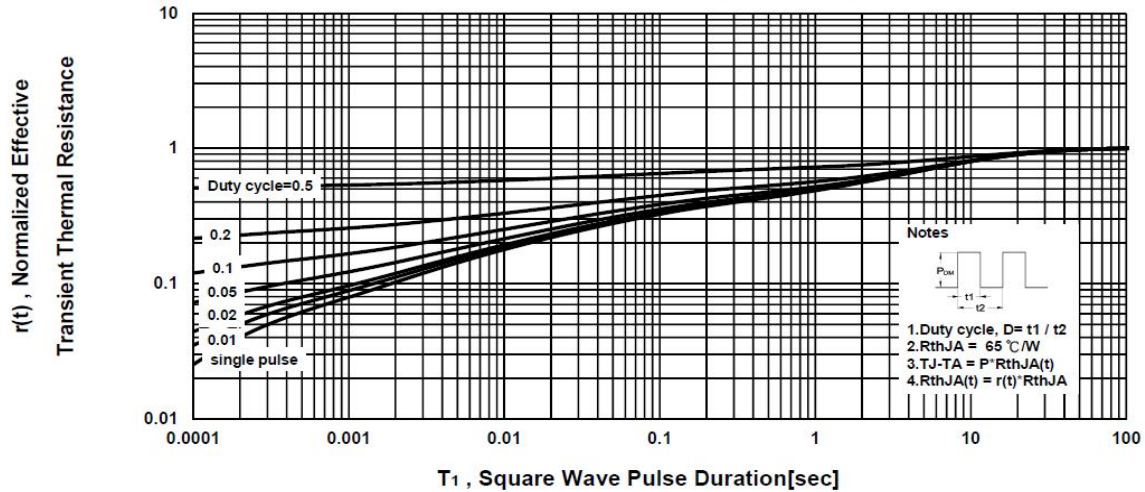
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**



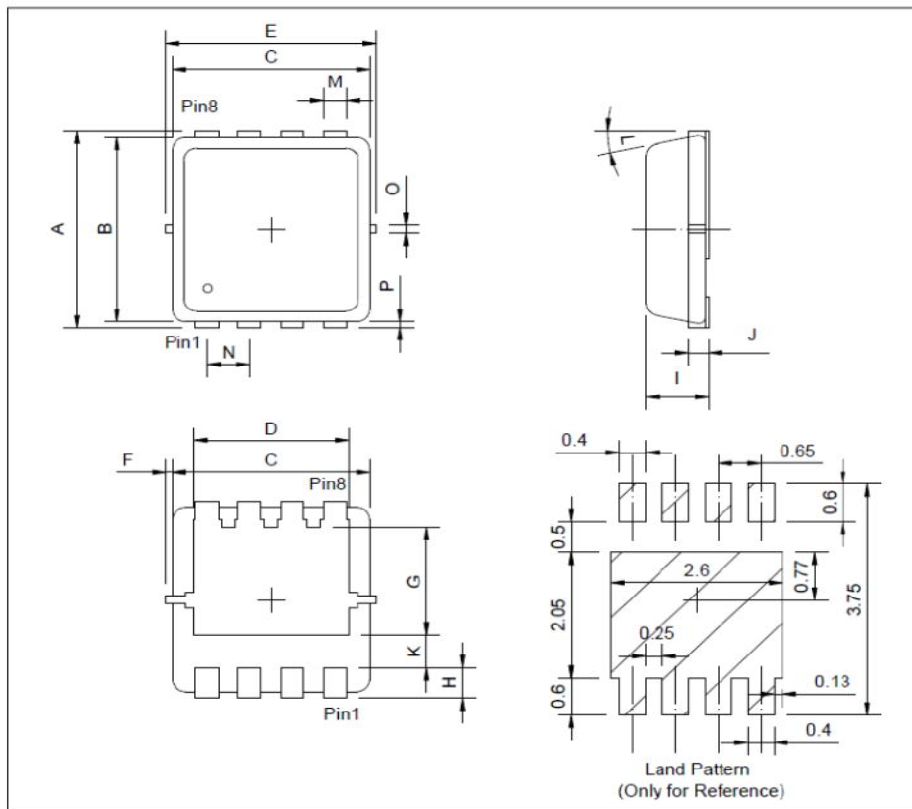
# PE551BA

## P-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### PDFN 3x3P MECHANICAL DATA

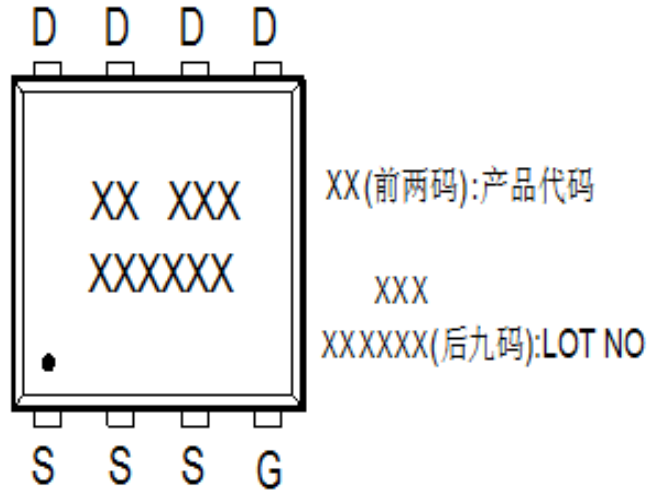
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	3	3.3	3.6	I	0.65	0.8	0.9
B	2.88	3	3.2	J	0.1	0.15	0.25
C	2.9	3	3.25	K	0.59		
D	2.29	2.45	2.69	L	0°	10°	12°
E	3	3.3	3.6	M	0.14	0.3	0.4
F	0	0.1	0.2	N	0.55	0.65	0.75
G	1.35	1.75	2.2	O		0.2	
H	0.15	0.3	0.55	P	0		0.2



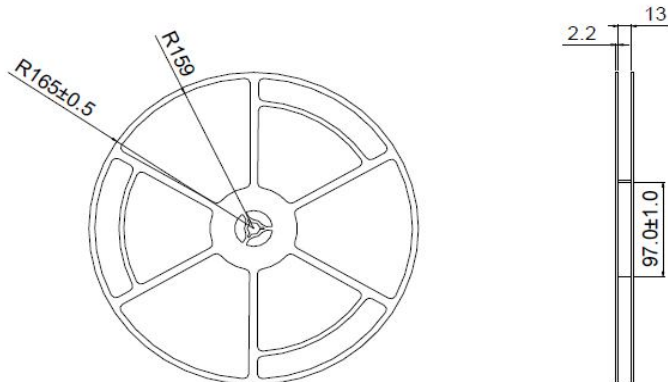
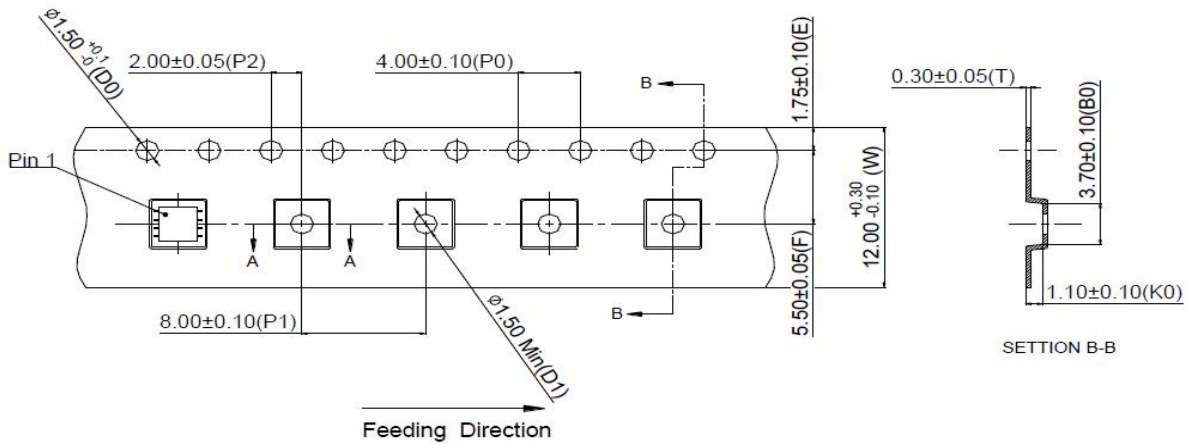
# PE551BA

## P-Channel Logic Level Enhancement Mode MOSFET

### A. Marking Information(此产品代码为: K1)



### B. Tape & Reel Information: 5000pcs/Reel

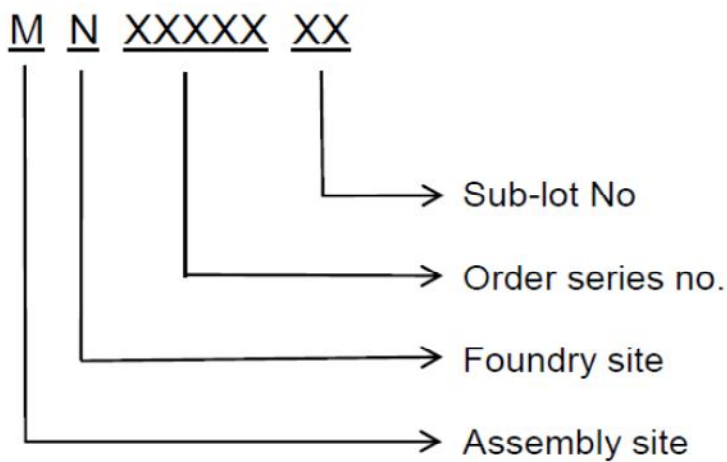


# PE551BA

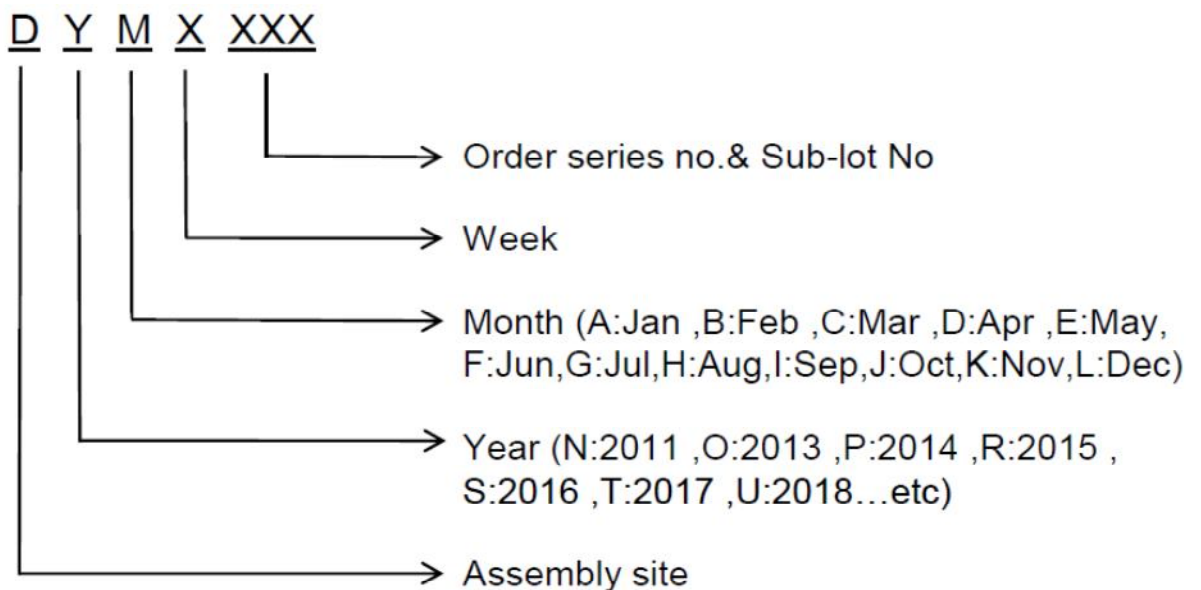
## P-Channel Logic Level Enhancement Mode MOSFET

### C. Lot No.&Date Code rule

#### 1.Lot No.



#### 2.Date Code







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## P-Channel Logic Level Enhancement Mode MOSFET

### D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert " / " between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least